Syllabus & Scheme for

M.Tech. (VLSI Design)

Department of Electronics Engineering

YMCA University of Science & Technology,

Faridabad (Haryana)

Total credit requirement of the course : 71 Max. Marks:2250
Core Courses : 10 Labs :06
Electives Courses : 02 Seminar :01
Project / Dissertation : 02

First Semester

Subject Code	Title	Credit (L-T-P)		Marks Weightage Theory	Sessional
E 601 V	Physics of Semiconductor Devices	4	4-0-0	60	40
E 603 V	Digital VLSI Design	4	4-0-0	60	40
E 605 V	Hardware Description Language for VLSI	4	4-0-0	60	40
E 607 V	Embedded System Design I	4	4-0-0	60	40
				External	Internal
E 609 V	Embedded System Lab-I	1	0-0-2	20	30
E 611 V	Digital VLSI Design Lab	1	0-0-2	20	30
E 613 V	HDL Lab	1	0-0-2	20	30
	Total	**19**	**16-0-6**	**300**	**250**

Instruction:
1.Sessional will be awarded by the teacher in marks only.
2.Theory paper will be awarded in marks.
3.Combining the theory and sessional marks university will compute percentage of marks in that subject.
4. On the basis of combined percentage of marks in a particular paper, the grade will be allocated according to the minutes of the BOS meeting held on 22/05/2010.

Second Semester

Subject Code	Title	Credit (L-T-P)		Marks Weightage Theory	Sessional
E 602 V	**Analog VLSI Design**	**4**	**4-0-0**	**60**	**40**
E 604 V	**IC Fabrication Technology**	**4**	**4-0-0**	**60**	**40**
E 606 V	**Embedded System Design-II**	**4**	**4-0-0**	**60**	**40**
E 608 V	**ASICs and FPGAs**	**4**	**4-0-0**	**60**	**40**
				External	**Internal**
E 610 V	**Analog VLSI Lab**	**1**	**0-0-2**	**20**	**30**
E 612 V	**Embedded System Lab -II**	**1**	**0-0-2**	**20**	**30**
E 614 V	**Seminar**	**1**	**0-0-2**	**--**	**50**
	Total	**19**	**16-0-6**	**280**	**270**

Instruction:
1. Sessional will be awarded by the teacher in marks only.
2. Theory paper will be awarded in marks.
3. Combining the theory and sessional marks university will compute percentage of marks in that subject.
4. On the basis of combined percentage of marks in a particular paper, the grade will be allocated according to the minutes of the BOS meeting held on 22/05/2010.

Third Semester

Subject Code	Title	Credit (L-T-P)	Marks Weightage Theory	Sessional
E 701 V	**Advanced Digital Signal Processing**	**4 4-0-0**	**60**	**40**
E 703 V	**Nanotechnology**	**4 4-0-0**	**60**	**40**
E 705 V	**Elective-I**	**4 4-0-0**	**60**	**40**
E 707 V	**Elective-II**	**4 4-0-0**	**60**	**40**
			External	**Internal**
E 709 V	**Minor Project**	**4 0-0-4**	**80**	**120**
E 711 V	**ADSP lab**	**1 0-0-2**	**20**	**30**
	Total	**21 16-0-10**	**340**	**310**

Fourth Semester

Subject Code	Title	Credit (L-T-P)	Marks Weightage Theory	Sessional
E 702 V	**Dissertation**	**12 0-0-24**	**200**	**300**
	Total	**12 0-0-24**	**200**	**300**

Instruction:
1.Sessional will be awarded by the teacher in marks only.
2.Theory paper will be awarded in marks.
3.Combining the theory and sessional marks university will compute percentage of marks in that subject.
4. On the basis of combined percentage of marks in a particular paper, the grade will be allocated according to the minutes of the BOS meeting held on 22/05/2010.

Elective - I

Sr. No.	Subject Code	Title
1	E 705(A) V	VLSI Architecture
2	E 705(B) V	Embedded Control System
3	E 705(C) V	Mixed signal Embedded System
4	E 705(D) V	CAD system Environment

Elective – II

Sr. No.	Subject Code	Title
1.	E 707(A) V	VLSI Testing and Design for Testability
2.	E 707(B) V	Low Power VLSI design
3	E 707(C) V	CAD for VLSI
4	E 707(D) V	Algorithm for VLSI Design Automation

Semester I

Physics of Semiconductor Devices

Semiconductor Electronics: Physics of Semiconductor Materials, Drift Velocity, Mobility, Scattering, Diffusion current, Band Model.

Metal Semiconductor Contacts: Metal-Semiconductor System, (V-I) and (C-V) equations for a Shottky - Barrier - Diode, Diode Construction, Device analysis using surface - states, applications as mixer and detectors in microwave region, Ohmic Contacts, Surface effects.

PN Junctions: Step junction, Linearly Graded Junction, (V-I) and (C-V) characteristics, Junction Breakdown, tunneling effect, avalanche multiplication, transient behaviour and noise. Use of junction diode as a rectifier, Voltage regulator, resistor varactor and fast recovery diode.

Bipolar Junction Transistors: Transistor action, Current -Voltage equation, output characteristics, breakdown voltage, Ebers-Moll and Gummel - Poon Model, early effect, Charge control model, small-signal transistor model, Simulation model,

Metal-oxide-silicon System: MOS structure, Energy Band Diagrams, Interface charges, Surface effects, MOS Capacitors.

MOS Transistors: Basic Theory, structure and operation, MOSFET parameters, Threshold Voltage and its control, Geometric effects on threshold, Ion-Implanted MOSFETs, Complementary MOSFET, Sub-threshold Conduction, velocity saturation, hot carriers, small geometry considerations

TEXT BOOKS:

1. S. M. Sze, *Modern Semiconductor Device Physics*, Wiley, 1998.
2. R. S. Muller and T. I. Kaminis, *Device Electronics for Integrated Circuits*, Second Edition, Wiley, 1986.

REFERENCE BOOKS:

1. B. G. Streetman, *Solid State Electronic Devices*, Fourth Edition, PH, 1995.
2. D. Foty, *MOSFET Modeling with SPICE : Principles and Practices*, PH, 1997.
3. P. W. Tuinenga, *SPICE : A Guide to Circuit Simulation and Analysis Using P-SPICE*, Third Edition, PH, 1995.
4. P. Antognetti and G. Massobrio, *Semiconductor Device and Modeling with SPICE*, Second Edition, MH, 1993.
5. T. A. Fjeldly, T. Ytterdal and M. Shur, *Introduction to Device Modeling and Circuit Simulation*, Wiley, 1997.
1. D. Nagchoudhuri, *Microelectronic Devices*, Pearson, 2001.
6. R. Raghuram, *Computer Simulation for Electronic Circuits*, Wiley, 1989.
7. G. W. Roberts and A. S. Sedra, *SPICE*, Second Edition, OUP, 1996.
8. A. S. Sedra and K. C. Smith, *Microelectronic Circuits*, Fourth Edition, OUP, 1997.
9. M. Shur, *Introduction to Electronic Devices*, Wiley, 1995.
10. M. Shur, *Physics of Semiconductor Devices*, PH, 1990.
11. M. S. Tyagi, *Introduction to Semiconductor Materials and Devices*, Wiley, 1991.
12. S. M. Sze, *Physics of Semiconductor Devices*, Second Edition, Wiley, 1981.
13. S. M. Sze, *Semiconductor Devices : Physics and Technology*, Wiley, 1985.
14. W. Liu, *MOSFET Models for SPICE Including BSIM3v3 and BSIM4*, Wiley, 2001.
15. Y. Cheng and C. Hu, *MOSFET Modeling and BSIM3 User's Guide*, Kluwer, 1999.
16. M. Satyam and K. Ramkumar, *Foundations of Electronic Devices*, Wiley, 1990.

Digital VLSI Design (E603V)

UNIT I REVIEW OF MOS TECHNOLOGY
Evolution of VLSI technology, VLSI Design Flow, Basic MOS Transistor: Enhancement and depletion mode, MOS structure, NMOS, PMOS and CMOS fabrication.

UNIT II ELECTRICAL PROPERTIES OF MOS
Threshold voltage, MOSFET current voltage characteristics, second order effects, MOS inverters: VTC characteristics of NMOS inverter, CMOS inverter and Bi-CMOS inverter. Noise margins, Latch-up in CMOS circuits.

UNIT III DESIGN PROCESS
Physical design of simple and complex logic gates using NMOS and CMOS technology, Stick diagrams, NMOS Design Style. CMOS Design Style, Lambda based Design Rules. Layout.

UNIT IV MOS TRANSISTOR SWITCHING CHARACTERISTICS
Sheet resistance, area capacitance, inverter delay. Switching power dissipation of CMOS inverters.

UNIT V DYANAMIC LOGIC CIRCUITS
CMOS Logic Structure: Complementary CMOS Logic, Pseudo NMOS Logic, Dynamic CMOS Logic, CMOS Domino Logic, Clocked CMOS Logic, Pass Transistor Logic, CMOS transmission gate Logic

UNIT VI SCALING OF MOS CIRCUITS
Scaling models, scaling factor for device parameters, Advantages and Limitations of scaling.

UNIT VII SUBSYSTEM DESIGN
Architectural issues in VLSI, Design of CMOS parity generator, Multiplexer, n-Bit Comparator, Incrementer/Decrementer, ALU subsystem.

TEXT BOOKS:
1. Kang and Leblebici “CMOS Digital integrated circuits” TMH 2003.
2. Pucknell D.A and Eshrachain K. “Basic VLSI Design Systems & circuits”(PHI)
3. Introduction to Digital Circuits: Rabaey (PH)

Hardware Description Languages for VLSI

Introduction To Hardware Design : Digital System Design Process, Hardware Description Languages, Hardware Simulation, Hardware Synthesis, Levels of Abstraction.

VHDL Background : VHDL History, Existing Languages, VHDL Requirements, The VHDL Language.

Design Methodology Based On VHDL : Elements of VHDL, Top down Design, Top down Design with VHDL, Subprograms, VHDL Operators, Conventions and Syntax.

Basic Concepts In VHDL : Characterizing Hardware Languages, Objects and Classes, Signal Assignments, Concurrent and Sequential Assignments.

Design Organization : Definition and Usage of Subprograms, Packaging Parts and Utilities, Generic and configuration, Design Configuration and Libraries.

Utilities For High-Level Descriptions : Type Declarations , VHDL Operators, Subprogram Parameter Types and Overloading, Predefined Attributes, User Defined Attributes.

Behavioral Description Of Hardware : Process Statement, Assertion Statement, Sequential Wait Statements.

Verilog: Overview of Digital design with Verilog HDL, basic concepts, modules & ports.

TEXT BOOKS:

1. J. Bhasker, *A VHDL Primer*, Third Edition, PH/Pearson, 1999.
2. J. Bhasker, *A VHDL Synthesis Primer*, Second Edition, Star Galaxy, 1998.
3. J. Bhasker, *A Verilog HDL Primer*, Second Edition, Star Galaxy, 1999.
4. J. Bhasker, *A Verilog Synthesis : A Practical Primer*, Star Galaxy, 1998.
5. M. J. S. Smith, *Application Specific Integrated Circuits*, AW/Pearson, 1997.

REFERENCE BOOKS:

1. Z. Navabi, *VHDL : Analysis and Modeling of Digital Systems*, Second Edition, MH, 1998..
2. J. Armstrong and F. G. Gray, *VHDL Design Representation and Synthesis*, Second Edition, PH/Pearson, 2000.
3. P. J. Ashenden, *The Designer's Guide to VHDL*, Second Edition, Morgan Kaufmann, 2001.
4. D. Naylor and S. Jones, *VHDL : A Logic Synthesis Approach*, Chapman & Hall, 1997.
5. J. Pick, *VHDL : Techniques, Experiments and Caveats*, MH, 1996.
6. C. H. Roth, *Digital System Design with VHDL*, PWS/Brookscole, 1998.
7. M. G. Arnold, *Verilog Digital Computer Design : Algorithms to Hardware*, PH, 1999.
8. Z. Navabi, *Verilog Digital System Design*, MH, 1999.
9. S. Palnitkar, *Verilog HDL : A Guide to Digital Design and Synthesis*, PH/Pearson, 1996.
10. D. E. Thomas and P. R. Moorby, *The Verilog Hardware Description Language*, Fourth Edition, Kluwer, 1998.
11. K. Coffman, *Real World FPGA Design with Verilog*, PH, 2000.
12. D. R. Smith and P. D. Franzon, *Verilog Styles for Synthesis of Digital Systems*, AW/Pearson, 2001.
13. S. M. Trimberger, *FPGA Technology*, Kluwer, 1992.
14. J. V. Oldfield and R. C. Dorf, *FPGAs : Reconfigurable Logic for Rapid Prototyping and Implementation of Digital Systems*, Wiley, 1995.
15. R. C. Seals and G. F. Whapshott, *Programmable Logic : PLDs and FPGAs*, MH, 1998.
16. A. K. Sharma, *Programmable Logic Handbook : PLDs, CPLDs and FPGAs*, MH, 1998.

Embedded System-I

MICROCONTROLLER 8051

Introduction, 8051 architecture and programming model. Internal RAM and registers, I/O ports, Interrupt system

PROGRAMMING WITH 8051

Jump, Loop and Call instructions, I/O port programming, Addressing modes, Arithmetic Instructions and programs Logic Instructions and programs, Single bit Instructions. Assembly Language Programming, Programming in C Language.

PERIPHERALS & INTERFACING

Timers and counters Serial Communications, Interrupts programming, Interfacing LCD, ADC and sensors, Interfacing stepper motors, keyboards and DAC'S.Interfacing external memory and 8255

MOTOROLA 68HC11 MICROCONTROLLER

Instructions and addressing modes – operating modes – Hardware reset, Interrupt system, Parallel I/O ports – Flats – Real time clock – Programmable timer – pulse accumulator, Serial communication interface – A/D converter – hardware expansion – Basic Assembly Language programming.

REAL TIME OPERATING SYSTEM

Real time operating system overview, Exposure to Windows CE, QNX, Micro kernels and pc/US of introduction to process models. Interrupt routines in an RTOS environment. Encapsulation semaphores and queues, hard real-time scheduling considerations, saving memory space.

Books :

1. Kenneth Ayala "The 8051 Micro controller Architecture, programming and Application" Penram Publication
2. M.A. Mazizi & J.G. Mazidi, The 8051 Micro controller:, Pearson Education
3. Gene. H.Miller, "Micro Computer Engineering", Pearson Education, 2003.
4. Rajkamal , "Embedded System Design" Tata McGrawHill

Semester II

Analog VLSI Design

Small Signal & large signal Models of MOS & BJT transistor. Analog MOS Process

MOS & BJT Transistor Amplifiers : Single transistor Amplifiers stages: Common Emitter, Common base, Common Collector, Common Drain, Common Gate & Common Source Amplifiers

Multiple Transistor Amplifier stages: CC-CE, CC-CC, & Darlington configuration, Cascode configuration, Differential Amplifiers: Differential pair & DC transfer characteristics.

Current Mirrors, Active Loads & References
Current Mirrors: Simple current mirror, Cascode current mirrors, Widlar current mirror, Wilson Current mirror, etc. Active loads, Voltage & current references. Analysis of Differential Amplifier with active load, supply and temperature independent biasing techniques, Frequency Response.

Operational Amplifier: Applications of operational Amplifier, theory and Design; Definition of Performance Characteristics; Design of two stage MOS Operational Amplifier, two stage MOS operational Amplifier with cascodes, MOS telescopic-cascode operational amplifiers, MOS Folded-cascode operational amplifiers, Frequency response & compensation.

Nonlinear Analog Circuits:
Digital-to-Analog (D/A) and Analog-to-Digital (A/D) Converters, Voltage controlled oscillator, Comparators, Phase Locked Loops (PLL)

OTA & Switched Capacitor filters
OTA Amplifiers. Switched Capacitor Circuits and Switched Capacitor Filters.

Text:

1. Paul B Gray and Robert G Meyer, “Analysis and Design of Analog Integrated Circuits”.
2. R Gregorian and G C Temes, Analog MOS Integrated Circuits for Signal Processing, John Wiley, 1986.
3. Allen and Holberg , “CMOS Analog Circuit Design” oxford University Press

References:

1. D. A. Johns and Martin, Analog Integrated Circuit Design, John Wiley, 1997.
2. R Gregorian and G C Temes, Analog MOS Integrated Circuits for Signal Processing, John Wiley, 1986.
3. Behzad Razavi, “Principles of data conversion system design”, S.Chand and company Ltd, 2000. John Wiley
4. Kenneth R. Laker, Willy M.C. Sensen, “ Design of Analog Integrated circuits and systems”, McGraw Hill, 1994.

IC Fabrication Technology

Environment for VLSI Technology : Clean room and safety requirements. Wafer cleaning processes and wet chemical etching techniques.

Impurity incorporation: Solid State diffusion modelling and technology; Ion Implantation modelling, technology and damage annealing; characterisation of Impurity profiles.

Oxidation : Kinetics of Silicon dioxide growth both for thick, thin and ultrathin films. Oxidation technologies in VLSI and ULSI; Characterisation of oxide films; High k and low k dielectrics for ULSI.

Lithography : Photolithography, E-beam lithography and newer lithography techniques for VLSI/ULSI; Mask generation.

Chemical Vapour Deposition techniques : CVD techniques for deposition of polysilicon, silicon dioxide, silicon nitride and metal films; Epitaxial growth of silicon; modelling and technology.

Metal film deposition : Evaporation and sputtering techniques. Failure mechanisms in metal interconnects; Multi-level metallisation schemes.

Plasma and Rapid Thermal Processing: PECVD, Plasma etching and RIE techniques; RTP techniques for annealing, growth and deposition of various films for use in ULSI.
Recent Trends in Fabrication, Process integration for NMOS, CMOS and Bipolar circuits; Advanced MOS technology.

Texts/References:

1. S.K. Ghandhi, VLSI Fabrication Principles, John Wiley Inc., New York, 1994(2^{nd} Edition).
2. S.M. Sze (Ed), VLSI Technology, 2nd Edition, McGraw Hill, 1988.
3. Plummer, Deal , Griffin “Silicon VLSI Technology: Fundamentals, Practice & Modeling” PH, 2001.
4. P. VanZant , “Microchip Fabrication”, 5^{th} Edition, MH , 2000.

ASICs and FPGAs

Introduction: course outline, logistics introduction to ASICs, FPGAs, economics

HDL: Logic design Review, Behavior, dataflow, structural modeling, control statements, FSM modeling

CMOS Review: Classical, CMOS (Deep Sub-micron), ASIC Methodologies

Fabrication of MOSFET: MOS Transistor, Design methodologies, design for testability.

FPGA: Programmable logic FPGA, Configuration logic blocks, Function Generator, ROM implementation, RAM implementation, time skew buffers, FPGA Design tools, Network-on-chip, Adaptive System-on-chip, AES ASIC Implementation, Advanced FPGA Design

Logic synthesis: Fundamentals, logic synthesis with synopsis, physical design compilation, simulation, implementation. V Floor planning and placement, Commercial EDA tools for synthesis.

Testing: Advanced interconnects and testing techniques

Text / Reference Books:

1. Bushnell and Agarwal “Essentials of Electronic Testing” KLUWER Academic Publishers.

Embedded System Design-II

THE PIC MICROCONTROLLER ARCHITECTURE

CPU, ALU , Data Movement, The Program Counter and Stack, Reset , Interrupts, Architecture Differences, Mid-Range instruction Set

PIC HARDWARE FEATURES

Power Input and Decoupling , Reset, Watchdog Timer, System Clock/Oscillators, Configuration Registers, Sleep , Hardware and File Registers, Parallel Input Output, Interrupts, Prescaler , The OPTION Register , Mid-Range Built-In EEPROM Flash Access, TMR1 andTMR2 Serial I/0, Analog I/0, Parallel Slave Port (PSP), External Memory Connections , In-Circuit Serial Programming (ISCP)

PROGRAMMING WITH PIC

Assembly Language Programming, Hex File Format, Code-Protect Features, Programming, PIC Emulators

HARDWARE LNTERFACING

Estimating Application Power Requirements, Reset, lnterfacing to External Devices, LEDs, Switch Bounce , Matrix Keypads , LCDs, Analog I/O, Relays and Solenoids, DC and Stepper Motors, Servo Control Serial Interfaces

ARM PROCESSOR FUNDAMENTALS

Registers, State and Instruction Sets, Pipeline, Memory Management, Introduction to the ARM Instruction Set

Books

1. Programming and customizing PIC microcontroller- Myke Predko, Mc- Graw Hill.
2. John.B. Peatman, “Design with PIC Micro controller”, Pearson Education, 2003.
3. Steave Furber, “ARM system – on – chip architecture” Addison Wesley, 2000.

Semester III

Advanced Digital Signal Processing

1. Introduction of DSP: Introduction to Signal Processing, Discrete Linear Systems, superposition Principle, Unit-Sample response, stability & causality Criterion.

2. Fourier Transform & inverse Fourier transform: Frequency domain design of digital filters, Fourier transform, use of Fourier transform in Signal processing. The inverse fourier transform, Sampling continuous function to generate a sequence, Reconstruction of continuous -time signals from Discrete-time sequences.

3. DFT & FFT & Z transform with Applications: Discrete Fourier transform, properties of DFT, Circular Convolution, Fast Fourier Transform, Realizations of OFT. The Ztransform, the system function of a digital filter, Digital Filter implementation from the system function, the inverse Z- transform, properties & applications, Special computation of finite sequences, sequence of infinite length & continuous time signals, computation of fourier series & time sequences from spectra.

4. Digital Filter Structure & Implementation: Linearity, time- invariance & causality, the discrete convolution, the transfer function, stability tests, steady state response, Amplitude & Phase characteristics, stabilization procedure, Ideal LP Filter, Physical reliability & specifications.FIR Filters, Truncation windowing & Delays, design example, IIR Filters:
Review of design of analog filters & analog frequency transformation. Digital frequency transformation. Design of LP filters using impulse invariance method, Bilinear transformation, Phase equalizer, digital all pass filters.

5. Implementation of Filters: Realization block diagrams, Cascade & parallel realization, effect of infinite-word length, transfer function of degree 1&2, Sensitivity comparisons, effects of finite precision arithmetic on Digital filters.

TextBooks

1 Alam V. Oppenheim & Ronald W. Schafer, "Digital Signal Processing" PHI.
2 JG Proakis, "Digital Signal Processing", (PHI) 3rd Edition.

Reference Books

I. Rabiner & Gold, "Theory & application of digital Signal Processing", PHI 1992. 2. Roman kuc, "Introduction to Digital Signal Processing," McGraw hill Edition.

Nanotechnology

Unit - I Atomic structure

Basic crystallography, Crystals and their imperfections, Diffusion, Nucleation and crystallization, Metals, Semiconductors and Insulators, Phase transformations , Ceramic materials.

Unit – II Physical Properties of Materials

Electrical and Thermal properties, Optical properties of materials, Magnetic properties of materials, Density of states, Coulomb blockade, Kondo effect,Hall effect,Quantum Hall Effect.

Unit – III Nanostructures

Introduction to Nanotechnology, Zero dimensional nanostructures – Nano particles, One dimensional nanostructures – Nano wires and Nano rods, Two dimensional nanostructures – Films, Special nano materials, Nano stuctures fabricated by Physical Techniques, Properties of Nanomaterials, Applications of Nano structures, Basics of Nano Electronics.

Unit – IV Characterization of Nanomaterials

SPM Tecniques – Scanning Tunneling Microscopy, Atomic Force Microscopy, Magnetic Force Microscopy, Electron Microscopy – Scanning Electron Microscope, Transmission Electron Microscope

Reference Books ;

1.Introduction to solid state Physics : C.Kittel
2. Introduction to theory of solids : H.M. Roenberg
3. Physics and Chemistry of materials : Joel I. Gersten
4.Handbook of Nanotechnology : Bharat Bhushan(springer)

Elective I

VLSI Architectures

Parallel computer models: The state of computing, Classification of parallel computers, Multiprocessors and multicomputers, Multivector and SIMD computers.

Program and network properties: Conditions of parallelism, Data and resource Dependences, Hardware and software parallelism, Program partitioning and scheduling, Grain Size and latency, Program flow mechanisms, Control flow versus data flow, Data flow Architecture, Demand driven mechanisms, Comparisons of flow mechanisms

System Interconnect Architectures: Network properties and routing, Static interconnection Networks, Dynamic interconnection Networks, Multiprocessor system Interconnects, Hierarchical bus systems, Crossbar switch and multiport memory, Multistage and combining network.

Advanced processors: Advanced processor technology, Instruction-set Architectures, CISC Scalar Processors, RISC Scalar Processors, Superscalar Processors, VLIW Architectures, Vector and Symbolic processors

Pipelining: Linear pipeline processor, nonlinear pipeline processor, Instruction pipeline Design, Mechanisms for instruction pipelining, Dynamic instruction scheduling, Branch Handling techniques, branch prediction, Arithmetic Pipeline Design, Computer arithmetic principles, Static Arithmetic pipeline, Multifunctional arithmetic pipelines

Memory Hierarchy Design: Cache basics & cache performance, reducing miss rate and miss penalty, multilevel cache hierarchies, main memory organizations, design of memory hierarchies.

Multiprocessor architectures: Symmetric shared memory architectures, distributed shared memory architectures, models of memory consistency, cache coherence protocols (MSI, MESI, MOESI), scalable cache coherence, overview of directory based approaches, design challenges of directory protocols, memory based directory protocols, cache based directory protocols, protocol design tradeoffs, synchronization,

Scalable point –point interfaces: Alpha364 and HT protocols, high performance signaling layer.

Text:

1. Kai Hwang, “Advanced computer architecture”; TMH.
2. D. A. Patterson and J. L. Hennessey, “Computer organization and design,” Morgan Kaufmann, 2nd Ed.

References:

1. J.P.Hayes, “computer Architecture and organization”; MGH.

2. Harvey G.Cragon,”Memory System and Pipelined processors”; Narosa Publication.

3. V.Rajaranam & C.S.R.Murthy, “Parallel computer”; PHI.

4. R.K.Ghose, Rajan Moona & Phalguni Gupta, “Foundation of Parallel Processing”; Narosa Publications.

5. Kai Hwang and Zu, “Scalable Parallel Computers Architecture”; MGH.

6. Stalling W, “Computer Organisation & Architecture”;PHI.

7. D.Sima, T.Fountain, P.Kasuk, “Advanced Computer Architecture-A Design space Approach,”Addison Wesley,1997.

Embedded Control System

INTRODUCTION

Controlling the hardware with software – Data lines, Address lines, Ports – Schematic representation – Bit masking – Programmable peripheral interface – Switch input detection – 74 LS 244

INPUT-OUTPUT DEVICES

Keyboard basics – Keyboard scanning algorithm – Multiplexed LED displays – Character LCD modules, LCD module display, Configuration – Time-of-day clock – Timer manager - Interrupts - Interrupt service routines, IRQ, ISR, Interrupt vector or dispatch table multiple-point - Interrupt-driven pulse width modulation.

D/A AND A/D CONVERSION

R 2R ladder - Resistor network analysis - Port offsets - Triangle waves analog vs. digital values - ADC0809 – Auto port detect - Recording and playing back voice - Capturing analog information in the timer interrupt service routine - Automatic, multiple channel analog to digital data acquisition.

ASYNCHRONOUS SERIAL COMMUNICATION

Asynchronous serial communication – RS-232, RS-485 – Sending and receiving data – Serial ports on PC – Low-level PC serial I/O module, Buffered serial I/O.

CASE STUDIES: EMBEDDED C PROGRAMMING

Multiple closure problems – Basic outputs with PPI – Controlling motors – Bi-directional control of motors – H bridge – Telephonic systems – Stepper control – Inventory control systems.

TEXT BOOKS:

1. Jean J. Labrosse, “Embedded Systems Building Blocks: Complete and Ready-To-Use Modules in C”, The publisher, Paul Temme, 2003.
2. Ball S.R., ‘Embedded microprocessor Systems – Real World Design’, Prentice Hall, 2001.

REFERENCE BOOKS:

1. Herma K, “Real Time Systems – Design for distributed Embedded Applications”, Kluwer Academic, 2003.
2. Daniel W. Lewis, “Fundamentals of Embedded Software where C and Assembly meet”, PHI, 2002.

Mixed Signal Embedded System

INTRODUCTION TO SYSTEM DESIGN

Dynamic Range, Calibration, Bandwidth, Processor Throughput, Avoiding Excess Speed , Other System Considerations, Sample Rate and Aliasing

DAC & ADC

Introduction - Nyqusist rate converters – Over sampling converters - Pipelined/parallel converters - High speed ADC design, High speed DAC design and Mixed signal design for radar application - ADC and DAC modules used for LIGO.

PLL

Introduction - Frequency Synthesizers - Design of PLL and Frequency Synthesizers – PLL with voltage driven oscillator – PLL with current driven oscillator – ETPLL – PLL synthesizer oscillator by MC14046B

SENSOR INTERFACING

Sensors, Sensor Types , Amplifier Design , Interfacing of Temperature, Pressure, Displacement Transducer in Embedded System Environment

LCD AND INFRA RED

LCD Fundamentals, Response Time, Temperature Effects, Connection Methods, Different types of LCD Panels, Static Waveforms, Infra Red Detection and Transmission

TIME-BASED MEASUREMENTS

Measuring Period versus Frequency , Mixing, Voltage-to-Frequency Converters, Clock Resolution and Range, Extending Accuracy with Limited Resolution

TEXT BOOKS:

1. Analog Interfacing to Embedded Microprocessors Real World Design, Stuart Ball.
2. Breems, “Continuous-Time Sigma Delta Modulations for A/D Conversion”,. Kluwer, 2002.

REFERENCE BOOKS:

1. Allen, “CMOS Analog Circuit Design”, Oxford, 2005.
2. Behzad Razavi, “Design of Analog CMOS integrated circuit”, Tata McGraw Hill, 2004.
2. Michelle Steyaert, “Analog Circuit Design”, Kluwer, 2003.
3. Gray & Meyer, Analysis and Design of Analog Integrated Circuits, Wiley, 2004.
4. Baker, CMOS Mixed-Signal Circuit Design, Wiley, 2004.

CAD System Environment

Familiarity with Unix/ Linux / Sun OS

Basic Concept of Operating System: Evolution of operating system, fundamental of operating system functions, multiprogramming, multiprocessing, time sharing systems and real time systems.

Linux : Brief History , Linux Distributions , Using the Emacs Editor , Using the vi Editor , Using the Pico Editor , Introduction to Users and Groups Essentials of Effective User, Group, and Password Management , Introduction to the Linux Kernel ,Using Kernel Modules ,Compiling the Linux Kernel ,Installing the Linux Kernel . File System , Disk Gemotary

UNIX: Familiarity with different shells ,UNIX Utilities like tar, make, yacc, lex, lint, debugger etc.Programming Tools : Perl, tcl/ tk File formats .tgz, .tar, X-term environment

SUN OS: The Solaris Operating Environment, Specific Features, Solaris Web Start Wizards, DHCP, Web-based enterprise management, Solaris Management Console, role-based access control (RBAC), Sun Management Center, Solaris Volume Manager, Solaris Resource Manager, Solaris Bandwidth Manager, Extensive Linux Compatibility

Windows NT,XP Environment

Familiarity with PVM: creating a parallel virtual environment, initiating server and daemons, PVM library routines, XPVM

Elective II

VLSI Testing and Design for Testability

Physical defects and their modeling; stuck at faults; Bridging Faults; Fault collapsing.

Fault Simulation: Deductive, Parallel and Concurrent; Critical Path Tracing.

Test Generation for Combinational Circuits: D-Algorithm, Boolean Difference, PODEM, and ATPG.

Random, Exhaustive and Weighted Random Test Pattern Generations Aliasing and its effect on Fault coverage.

PLA Testing: cross-point Fault Model, Test Generation,

Memory testing: Permanent Intermittent and Pattern Sensitive Faults; Delay Faults and Hazards; Test Generation Techniques;

Test Generation for Sequential Circuits.

Scan Design. Scan path and LSSD, BILBO

Concept of Redundancy, spatial redundancy, Time redundancy

Recent trends in VLSI testing: Genetic Algorithms, Parallel Algorithms, Neural networks, nano scale testing

Text books:

1. VLSI Testing: digital and mixed analogue digital techniques Stanley L. Hurst Pub:Inspec/IEE ,1999

Low Power VLSI Design

Low power Basics

Need for low power VLSI chips, Sources of power dissipation on Digital Integrated circuits. Emerging Low power approaches. Physics of power dissipation in CMOS devices.

Device & Technology Impact on Low Power

Dynamic dissipation in CMOS, Transistor sizing & gate oxide thickness, Impact of technology Scaling, Technology & Device innovation.

Power estimation

Simulation Power analysis: SPICE circuit simulators, gate level logic simulation, capacitive power estimation, static state power, gate level capacitance estimation, architecture level analysis, data correlation analysis in DSP systems. .

Low Power Design

Circuit level: Power consumption in circuits. Flip Flops & Latches design, high capacitance nodes, low power digital cells library **Logic level:** Gate reorganization, signal gating, logic encoding, state machine encoding, pre-computation logic

Low power Architecture & Systems: Power & performance management, switching activity reduction, parallel architecture with voltage reduction, flow graph transformation, low power arithmetic components, low power memory design.

Low power Clock Distribution: Power dissipation in clock distribution, single driver Vs distributed buffers, Zero skew Vs tolerable skew, chip & package co design of clock network

Algorithm & architectural level methodologies: Introduction, design flow, Algorithmic level analysis & optimization, Architectural level estimation & synthesis.

Text:

1. Gary K. Yeap, “Practical Low Power Digital VLSI Design”, KAP, 2002

2. Rabaey, Pedram, “Low power design methodologies” Kluwer Academic, 1997

References:

1. Kaushik Roy, Sharat Prasad, “Low-Power CMOS VLSI Circuit Design” Wiley, 2000

CAD for VLSI

Introduction to VLSI design methodologies and supporting CAD environment.

Schematic editors: Parsing: Reading files, describing data formats, Graphics & Plotting Layout. Layout Editor: Turning plotter into an editor. Layout language: Parameterized cells, PLA generators, Introduction to Silicon compiler, Datapath. Compiler, Placement & routing, Floor planning.

Layout Analysis: Design rules, Object based DRC, Edge based layout operations. Module generators.

Simulation: Types of simulation, Behavioral simulator, logic simulator, functional simulator & Circuit simulator.

Simulation Algorithms: Compiled code and Event-driven. Optimization Algorithms: Greedy methods, simulated annealing, genetic algorithm and neural models.

Testing ICs: Fault simulation, Aids for test generation and testing. Computational complexity issues: Big Oh and big omega terms.

Recent topics in CAD-VLSI: Array compilers, hardware software co-design, high-level synthesis tools and VHDL modeling.

Books:

1. Trimburger," Introduction to CAD for VLSI", Kluwer Academic publisher, 2002

2. Naveed Shervani, "Algorithms for VLSI physical design Automation", Kluwer Academic Publisher, Second edition.

Algorithms for VLSI Design Automation

VLSI physical design automation and Fabrication
VLSI Design cycle, New trends in VLSI design, Physical design cycle, Design style, Introduction to fabrication process, design rules, layout of basic devices

VLSI automation Algorithms:
Partitioning: problem formulation, classification of partitioning algorithms, Group migration algorithms, simulated annealing.

Floor planning & pin assignment: problem formulation, classification of floor planning algorithms, constraint based floor planning, floor planning algorithms for mixed block & cell design, chip planning, pin assignment, problem formulation, classification of pin assignment algorithms, General & channel pin assignment

Placement
Problem formulation, classification of placement algorithms, simulation base placement algorithms, recent trends in placement

Global Routing and Detailed routing: Problem formulation, classification of global routing algorithms, Maze routing algorithm, line probe algorithm, Steiner Tree based algorithms, performance driven routing
Detailed routing problem formulation, classification of routing algorithms, introduction to single layer routing algorithms, two layer channel routing algorithms, greedy channel routing, switchbox routing algorithms.

Over the cell routing & via minimization: two layers over the cell routers, constrained & unconstrained via minimization

Compaction: problem formulation, classification of compaction algorithms, one-dimensional compaction, two dimension based compaction, hierarchical compaction

Text Books:
1. Naveed Shervani, "Algorithms for VLSI physical design Automation", Kluwer Academic Publisher, Second edition.

References
1. Christophn Meinel & Thorsten Theobold, "Algorithm and Data Structures for VLSI Design", KAP, 2002.
2. Rolf Drechsheler : "Evolutionary Algorithm for VLSI", Second edition
3. Trimburger," Introduction to CAD for VLSI", Kluwer Academic publisher, 2002