SCHEME & SYLLABUS

for

M.TECH. COURSE

in

VLSI DESIGN

(w.e.f. Session 2017-2018)

DEPARTMENT OF ELECTRONICS ENGINEERING

YMCA UNIVERSITY OF SCIENCE AND TECHNOLOGY
FARIDABAD

VISION

YMCA University of Science and Technology aspires to be a nationally and internationally acclaimed leader in technical and higher education in all spheres which transforms the life of students through integration of teaching, research and character building.

MISSION

- To contribute to the development of science and technology by synthesizing teaching, research and creative activities.
- To provide an enviable research environment and state-of-the-art technological exposure to its scholars.
- To develop human potential to its fullest extent and make them emerge as world class leaders in their professions and enthuse them towards their social responsibilities.

Department of Electronics Engineering

VISION

To be a Centre of Excellence for producing high quality engineers and scientists capable of providing sustainable solutions to complex problems and promoting cost effective indigenous technology in the area of Electronics, Communication & Control Engineering for Industry, Research Organizations, Academia and all sections of society.

MISSION

- To frame a well-balanced curriculum with an emphasis on basic theoretical knowledge as well the requirements of the industry.
- To motivate students to develop innovative solutions to the existing problems for betterment of the society.
- Collaboration with the industry, research establishments and other academic institutions to bolster the research and development activities.
- To provide infrastructure and financial support for culmination of novel ideas into useful prototypes.
- To promote research in emerging and interdisciplinary areas and act as a facilitator for knowledge generation and dissemination through Research, Institute - Industry and Institute-Institute interaction.

About Electronics Engineering Department

YMCA University of Science & Technology, Faridabad established in 2009, formerly known as YMCA Institute of Engineering, Faridabad, established in year 1969 as a Joint Venture of Govt. of Haryana and National Council of YMCA of India with active assistance from overseas agencies of West Germany to produce highly practical oriented personnel in specialized field of engineering to meet specific technical manpower requirement of industries. Electronics Engineering Department started in 1969 and has been conducting B.Tech. Courses in Electronics Instrumentation and Control and Electronics and Communication Engineering of 4-Years duration since 1997. Students are admitted through centralized counseling nominated by state govt. in 1st Year and 2nd year through lateral entry entrance test. Besides under graduate degree courses, it is also running M.Tech. Courses in VLSI, Instrumentation and Electronics & Communication. Department of Electronics Engineering is also running Ph.D. Programme. All courses are duly approved by AICTE/ UGC. The Electronics Engineering Department has been well known for its track record of employment of the pass out students since its inception.

The Department has good infrastructure consisting of 11 laboratories, 10 Lecture Halls and 1 Conference Room beside 6 workshops. It has excellent faculty with 2 Professors, 2Associate Professors and 21 Assistant Professors. At present, 6 faculty members are PhD in various specializations. The various syllabi of UG/PG courses have been prepared with active participation from Industry. The Department is organizing number of expert lectures from industry experts for students in every semester. Seven month training is mandatory for every B.Tech. Students. Emphasis has been given on project work and workshop for skill enhancement of students. Choice based credit system allows students to study the subjects of his/her choice from a number of elective courses /audit courses.

Program Educational Objectives (PEO):

Students of the Master of Technology programs in VLSI Design will demonstrate

1. To educate and train the graduates with knowledge and skills necessary to formulate, design and solve problems in Analog, Digital & Mixed Signal VLSI system design, VLSI Signal Processing, Real Time Embedded System design and Hardware Software Co-Design.
2. To provide technical skills in software and hardware tools related to the design and implementation of integrated Circuits, System on Chip for real time applications.
3. To provide scope for Applied Research and innovation in the various fields of VLSI and Embedded Systems, and enabling the students to work in the emerging areas.
4. To enhance communication and soft skills of students to make them work effectively as a team

Program Outcomes (PO):

On successful completion of the Program, the students will be able to

1. Demonstrate in-depth knowledge in the specialized domain of Analog, Digital & Mixed Signal VLSI system design, VLSI Signal Processing, Real Time Embedded System design and Hardware Software Co-Design.
2. Analyze complex engineering problems critically in the domains of Analog, Digital & Mixed Signal VLSI system design, VLSI Signal Processing, Real Time Embedded System design and Hardware Software Co-Design for conducting research.
3. Solve engineering problems to arrive at optimal solutions in the fields of Analog and Digital VLSI complying with societal needs.
4. Apply appropriate research methodologies and techniques for the development of scientific and technological knowledge in Analog, Digital & Mixed Signal VLSI system design, VLSI Signal Processing, Real Time Embedded System design and Hardware Software Co-Design and Allied Areas.
5. Apply appropriate resources and modern tools to complex engineering activities in the field of VLSI and Embedded Systems.
6. Contribute to collaborative-multidisciplinary scientific work, demonstrate capacity for self-management, teamwork and decision making.

7. Manage projects as a member and leader with understanding of engineering and management principles with consideration to economic and financial factors.
8. Communicate effectively in professional and personal domains through verbal, written and graphical forms.
9. Engage in life-long learning to improve knowledge and competence in the world of rapid technological changes.
10. Follow ethical code of conduct in professional activities with understanding of responsibility for sustainable development of society.
11. Adapt to reflective self learning for continuous personal and professional development.
12. Participate and succeed in competitive examinations like GATE (for placements in PSU's), GRE (for higher studies).

M. TECH. (VLSI Design)

SCHEME AND SYLLABUS

Total Credits : 78

Total Theory Subjects : 12+1 (AC) + 1(GEC)+ 1(MOOCs)

Total Labs (including Seminars & Projects) : 08

Total Dissertation : 01

Total Teaching Schedule:

Lectures	Practical	Total
53	14	67

Total Marks:

Sessionals	End Term	Total
675	1675	2350

Itemised Break-up:

	No.	Hours	Marks	Credits
Theory Subjects	12+3*	54	1300	51+4(MOOCs)
Labs	6	12	300	6
Seminar	1	2	50	1
Project	1	4	200	4
Thesis	1	1 Semester	500	12
Total	21+3*		2350	74+4 (MOOCs)

*MOOCs+GEC+AC

Scheme of Studies & Examination
M.Tech. (VLSI Design)

First semester

Subject Code	Subject Title	Credit / (L-T-P)		Marks Weightage		Total (Theory +Sessional)
				Theory	Sessional	
E16V 601	Physics of semiconductor devices	4	4-0-0	75	25	100
E16V 603	Digital VLSI Design	4	4-0-0	75	25	100
E16V 605	Hardware Description language for VLSI	4	4-0-0	75	25	100
E16V 607	Embedded System design I	4	4-0-0	75	25	100
				External	Internal	
E16V 609	Embedded System Lab-I	1	0-0-2	35	15	50
E16V 611	Digital VLSI Design lab	1	0-0-2	35	15	50
E16V 613	HDL Lab	1	0-0-2	35	15	50
	Total	19	16-0-6	405	145	550

Second Semester

Subject Code	Subject Title	Credit / (L-T-P)		Marks Weightage		Total (Theory +Sessional)
				Theory	Sessional	
E16V 602	Analog VLSI Design	4	4-0-0	75	25	100
E16V 604	IC Fabrication Technology	4	4-0-0	75	25	100
E16V 606	Embedded System Design-II	4	4-0-0	75	25	100
	Elective –I*	4	4-0-0	75	25	100
	Audit Course	0	3-0-0	-	-	-
	MOOCs	4	0	-	-	-
				External	Internal	
E16V 610	Analog VLSI Lab	1	0-0-2	35	15	50
E16V 612	Embedded System Lab -II	1	0-0-2	35	15	50
E16V 614	Seminar	1	0-0-2	-	50	50
	Total	23	23-0-6	370	180	550

***The student will have to select a subject from list of elective as under.**

****passing the MOOCs course is compulsory as per UGC guidelines, these online courses can be registered on UGC website under "Swayam" program. Four credits for the MOOCS course are to be earned in any semester from II to IV.**

THIRD SEMESTER

Subject Code	Subject Title	Credit (L-T-P)		Marks Weightage		Total (Theory +Sessional)
				Theory	Sessional	
E16V 701	Advanced Digital Signal Processing	4	4-0-0	75	25	100
E16V 703	Nanotechnology	4	4-0-0	75	25	100
	Elective-II *	4	4-0-0	75	25	100
	Elective-III*	4	4-0-0	75	25	100
	General Elective Course	3	3-0-0	75	25	100
				External	Internal	
E16V 709	ADSP Lab	1	0-0-2	35	15	50
E16V 711	Minor Project	4	0-0-8	140	60	200
	Total	24	15-0-10	550	200	750

***The student will have to select a subject from list of elective as under**

FOURTH SEMESTER

Subject Code	Subject Title	Credit (L-T-P)		Marks Weightage	
				Final	Sessional
E16V 702	Dissertation	12	0-0-24	350	150
	Total	12	0-0-24	500	

***The student will have to select subject from list of elective as under**

List of Elective

Elective –I

i. ASICs and FPGA (E16V 608 A)
ii. CAD system Environment (E16V 608 B)
iii. CAD for VLSI (E16V 608 C)

Elective – II

i. VLSI Architecture (E16V 705 A)
ii. Embedded Control System (E16V 705 B)
iii. Mixed signal Embedded System (E16V 705 C)

Elective – III

i. VLSI Testing and Design for Testability (E16V 707 A)
ii. Low Power VLSI design (E16V 707 B)
iii. Algorithm for VLSI Design Automation (E16V 707 C)

Audit Course

S.No.	Code	Name of Course	No. of Contact Hours	Credits
1.	AC-101C	German- I	2	0
2.	AC-102C	German –II (With German – I as prerequisite)	2	0
3.	AC-103C	French – I	2	0
4.	AC-104C	French –II (With French – I as prerequisite)	2	0
5.	AC-105C	Sanskrit – I	2	0
6.	AC-106C	Sanskrit – II (With Sanskrit– I as prerequisite)	2	0
7.	AC-107C	Personality Development	2	0
8.	AC-108C	Interview and Group Discussion Skills	2	0
9.	AC-109C	Yoga and Meditation	2	0
10.	AC-110C	Art of Living/ Living Skills	2	0
11.	AC-111C	Contribution of NSS towards Nation/Role of NSS	2	0
12.	AC-112C	Physical Education	2	0

GENERAL ELECTIVE COURSES

Students have to select General Elective Course from the given list:

Courses offered by Computer Engineering Department

S.No.	Code	Name of Course	No. of Contact Hours	Credits
1.	GC-101C	Intelligent Systems	3	3
2.	GC-102C	Cyber laws and Security	3	3
3.	GC-103C	Soft Computing	3	3
4.	GC-104C	Web Technology and Information Retrieval	3	3
5.	GC-105C	Intellectual Property and Rights	3	3

Courses offered by Electrical Engineering Department

S.No.	Code	Name of Course	No. of Contact Hours	Credits
1.	GL-201C	Installation Testing & Maintenance of Electrical Equipments	3	3
2.	GL-202C	Utilization of Electrical Power & Traction	3	3

Courses offered by Mechanical Engineering Department :

S.No.	Code	Name of Course	No. of Contact Hours	Credits
1.	GM-301C	Industrial Engineering	3	3
2.	GM-302C	Quality Management	3	3
3.	GM-303C	Automobile Engineering	3	3
4.	GM-304C	CAM and Automation	3	3
5.	GM-305C	Manufacturing Processes	3	3
6.	GM-306C	Power Plant Engineering	3	3

Courses offered by Electronics Engineering Department

(Not for Electronics Engineering students):

S.No.	Code	Name of Course	No. of Contact Hours	Credits
1.	GE-401C	Microprocessor and Interfacing	3	3
2.	GE-402C	Digital Signal Processing	3	3
3.	GE-403C	Instrumentation and Control	3	3
4.	GE-404C	Data Communication and Networking	3	3

Courses offered by HAS Department

S.No.		Name of Course	No. of Contact Hours	Credits
1.	GA-501C	Soft Skills for Engineers	3	3
2.	GA-502C	Maths –III	3	3

Courses offered by MBA Department

S.No.		Name of Course	No. of Contact Hours	Credits
1.	GB-601C	Human Resource Management	3	3
2.	GB-602C	Financial Management	3	3
3.	GB-603B	Marketing Management	3	3
4.	GB-604B	Entrepreneur Development	3	3
5.	GB-605B	Principles of Management and Economics	3	3

Courses offered under Open Elective

The syllabus of open elective will be standard one taken from reputed Institute/University.

S.No.	Code	Name of Course	No. of Contact Hours	Credits
1.	GO-701C	Physical Education	3	3
2.	GO-702C	Indian History	3	3

3.	GO-703C	General Psychology	3	3
4.	GO-704C	Fundamentals of Linguistics Science	3	3
5.	GO-705C	Swami Vivekanand's Thoughts	3	3
6.	GO-706C	National Integration	3	3
7.	GO-707C	Moral Values	3	3

SESSIONAL MARKS

The allocation of theory and sessional weightage for end semester examination would be as under:-

1. **For Theory**
    a) Sessional Weightage 25%
    b) End Semester Exam 75%
2. **For Practical**

    a) Sessional Weightage 30%
    b) End Semester Exam 70%

The academic performance of a student shall be graded on a TEN-POINT SCALE and the awards for grades based upon marks obtained out of 100 shall be made as follow:

Marks %	Grade	Grade points	Category
90-100	**O**	**10**	**Outstanding**
80<marks<90	**A+**	**9**	**Excellent**
70<marks< 80	**A**	**8**	**Very good**
60<marks< 70	**B+**	**7**	**Good**
50<marks< 60	**B**	**6**	**Above average**
45<marks< 50	**C**	**5**	**Average**
40<marks< 45	**P**	**4**	**Pass**
<40	**F**	**0**	**Fail**
	Ab	**0**	**Absent**

Percentage calculation= CGPA * 9.5

E16V-601 **PHYSICS OF SEMICONDUCTOR DEVICES**

L T P CR			
4 0 0 4	**Theory**	**:**	**75**
	Class Work	**:**	**25**
	Total	**:**	**100**
	Duration of Exam	**:**	**3 Hrs.**

Course Objectives:

- To learn the Physics of Semiconductor Materials, Scattering, Diffusion current, Band Model.
- To study the Metal Semiconductor Contacts, Metal-Semiconductor System, (V-I) and (C-V) equations for a Shottky - Barrier - Diode, Surface effects.
- To learn Step junction, Linearly Graded Junction, (V-I) and (C-V) characteristics, Junction Breakdown, fast recovery diode.
- To study the Transistor action, Current -Voltage equation, Ebers-Moll and Gummel - Poon Model, Charge control model, small-signal transistor model, Simulation model.
- To study MOS structure, Energy Band Diagrams, Interface charges, Surface effects, MOS Capacitors.
- To learn MOSFET parameters, Threshold Voltage and its control, Geometric effects on threshold, Ion-Implanted MOSFETs , Sub-threshold Conduction, velocity saturation, hot carriers, small geometry considerations.

SYLLABUS

Semiconductor Electronics: Physics of Semiconductor Materials, Drift Velocity, Mobility, Scattering, Diffusion current, Band Model.

Metal Semiconductor Contacts: Metal-Semiconductor System, (V-I) and (C-V) equations for a Shottky - Barrier - Diode, Diode Construction, Device analysis using surface - states, applications as mixer and detectors in microwave region, Ohmic Contacts, Surface effects.

PN Junctions: Step junction, Linearly Graded Junction, (V-I) and (C-V) characteristics, Junction Breakdown, tunneling effect, avalanche multiplication, transient behaviour and noise. Use of junction diode as a rectifier, Voltage regulator, resistor varactor and fast recovery diode.

Bipolar Junction Transistors: Transistor action, Current -Voltage equation, output characteristics, breakdown voltage, Ebers-Moll and Gummel - Poon Model, early effect, Charge control model, small-signal transistor model, Simulation model,

Metal-oxide-silicon System: MOS structure, Energy Band Diagrams, Interface charges, Surface effects, MOS Capacitors.

MOS Transistors: Basic Theory, structure and operation, MOSFET parameters, Threshold Voltage and its control, Geometric effects on threshold, Ion-Implanted MOSFETs, Complementary MOSFET, Sub-threshold Conduction, velocity saturation, hot carriers, small geometry considerations

Course Outcomes: At the end of the course the students shall be able to:

- Understand the basic properties of semiconductors including crystal growth and structure, band structure, doping, carrier transport and recombination phenomena.
- Understand the basic the principles of the operation of p-n junction, including current-voltage characteristics, charge storage and transient behavior, junction breakdown and fast recovery diode.
- Understand the basic principles of the operation of bipolar junction transistors and various models.
- Understand the fundamentals of MOSFET and metal-semiconductor contacts and their applications.

TEXT BOOKS:

1. S. M. Sze, *Modern Semiconductor Device Physics*, Wiley, 1998.
2. R. S. Muller and T. I. Kaminis, *Device Electronics for Integrated Circuits*, Second Edition, Wiley, 1986.

REFERENCE BOOKS:

1. B. G. Streetman, *Solid State Electronic Devices*, Fourth Edition, PH, 1995.
2. D. Foty, *MOSFET Modeling with SPICE : Principles and Practices*, PH, 1997.
3. P. W. Tuinenga, *SPICE : A Guide to Circuit Simulation and Analysis Using P-SPICE*, Third Edition, PH, 1995.
4. P. Antognetti and G. Massobrio, *Semiconductor Device and Modeling with SPICE*, Second Edition, MH, 1993.
5. T. A. Fjeldly, T. Ytterdal and M. Shur, *Introduction to Device Modeling and Circuit Simulation*, Wiley, 1997.
6. D. Nagchoudhuri, *Microelectronic Devices*, Pearson, 2001.
7. R. Raghuram, *Computer Simulation for Electronic Circuits*, Wiley, 1989.
8. A. S. Sedra and K. C. Smith, *Microelectronic Circuits*, Fourth Edition, OUP, 1997.
9. M. Shur, *Introduction to Electronic Devices*, Wiley, 1995.
10. M. S. Tyagi, *Introduction to Semiconductor Materials and Devices*, Wiley, 1991.
11. S. M. Sze, *Physics of Semiconductor Devices*, Second Edition, Wiley, 1981.
12. W. Liu, *MOSFET Models for SPICE Including BSIM3v3 and BSIM4*, Wiley, 2001.
13. Y. Cheng and C. Hu, *MOSFET Modeling and BSIM3 User's Guide*, Kluwer, 1999.
14. M. Satyam and K. Ramkumar, *Foundations of Electronic Devices*, Wiley, 1990.

E16V-603 **DIGITAL VLSI DESIGN**

L T P CR			
4 0 0 4	**Theory**	**:**	**75**
	Class Work	**:**	**25**
	Total	**:**	**100**
	Duration of Exam	**:**	**3 Hrs.**

COURSE OBJECTIVE

- To study the evolution of VLSI technology, VLSI Design Flow, Basic MOS Transistor: Enhancement and depletion mode, MOS structure, NMOS, PMOS and CMOS fabrication.
- To study the electrical properties of MOS Threshold voltage, MOSFET current voltage characteristics, second order effects, MOS inverters: VTC characteristics of NMOS inverter, CMOS inverter and Bi-CMOS inverter. Noise margins, Latch-up in CMOS circuits.
- To study the design process of Physical design of simple and complex logic gates using NMOS and CMOS technology, Stick diagrams, NMOS Design Style. CMOS Design Style, Lambda based Design Rules. Layout.
- To study the MOS transistor switching characteristics, Sheet resistance, area capacitance, inverter delay. Switching power dissipation of CMOS inverters.
- To study the dynamic logic circuits CMOS Logic Structure, Complementary CMOS Logic, Pseudo NMOS Logic, Dynamic CMOS Logic, CMOS Domino Logic, Clocked CMOS Logic, Pass Transistor Logic, CMOS transmission gate Logic
- To study the scaling of MOS circuits,scaling models, scaling factor for device parameters, Advantages and Limitations of scaling.
- To study of subsystem design, Architectural issues in VLSI, Design of CMOS parity generator, Multiplexer, n-Bit Comparator, Incrementer/Decrementer, ALU subsystem

SYLLABUS

UNIT I REVIEW OF MOS TECHNOLOGY

Evolution of VLSI technology, VLSI Design Flow, Basic MOS Transistor: Enhancement and depletion mode, MOS structure, NMOS, PMOS and CMOS fabrication.

UNIT II ELECTRICAL PROPERTIES OF MOS

Threshold voltage, MOSFET current voltage characteristics, second order effects, MOS inverters: VTC characteristics of NMOS inverter, CMOS inverter and Bi-CMOS inverter. Noise margins, Latch-up in CMOS circuits.

UNIT III DESIGN PROCESS

Physical design of simple and complex logic gates using NMOS and CMOS technology, Stick diagrams, NMOS Design Style. CMOS Design Style, Lambda based Design Rules. Layout.

UNIT IV MOS TRANSISTOR SWITCHING CHARACTERISTICS

Sheet resistance, area capacitance, inverter delay. Switching power dissipation of CMOS inverters.

UNIT V DYANAMIC LOGIC CIRCUITS

CMOS Logic Structure: Complementary CMOS Logic, Pseudo NMOS Logic, Dynamic CMOS Logic, CMOS Domino Logic, Clocked CMOS Logic, Pass Transistor Logic, CMOS transmission gate Logic

UNIT VI SCALING OF MOS CIRCUITS

Scaling models, scaling factor for device parameters, Advantages and Limitations of scaling.

UNIT VII SUBSYSTEM DESIGN

Architectural issues in VLSI, Design of CMOS parity generator, Multiplexer, n-Bit Comparator, Incrementer/Decrementer, ALU subsystem.

COURSE OUTCOME

At the end of the course the students shall be able to:

- Understand the VLSI design flow, enhancement & depletion type transistors and fabrication of NMOS, PMOS & CMOS.
- Understand the electrical properties of MOS, VTC characteristics of NMOS inverter, CMOS inverter &BiCMOS inverter, Latch-up concept
- Design & working of logic circuits using NMOS & CMOS technology & also understanding the concept of stick diagram & layout. Understand the concept & derivations of MOS switching characteristics i.e sheet resistance, capacitance & power dissipation.
- Design of various dynamic circuits i.e Pseudo NMOS logic ,CMOS dynamic Logic etc & design of other complex structures using pass transistors & transmission gates. Understand the concept of scaling of MOS, Scaling factors & parameters.
- Understand the architectural issues to design any subsystem & design of multiplexer, comparator, ALU & other complex circuits.

TEXT BOOKS:

1. Kang and Leblebici "CMOS Digital integrated circuits" TMH 2003.
2. Pucknell D.A and Eshrachain K. "Basic VLSI Design Systems & circuits"(PHI)
3. Introduction to Digital Circuits: Rabaey (PH)

E16V-605 HARDWARE DESCRIPTION LANGUAGES FOR VLSI

L T P CR			
4 0 0 4	**Theory**	**:**	**75**
	Class Work	**:**	**25**
	Total	**:**	**100**
	Duration of Exam	**:**	**3 Hrs.**

COURSE OBJECTIVE

1. To introduce VHDL background and Design methodology based on VHDL

2. To learn modeling of digital systems using VHDL.

3. To learn the basics of sequential and concurrent techniques in VHDL.

4. To explain data types, subprograms, packages, predefined attributes and configurations of VHDL.

5. To understand simulation and test bench creation.

6. To introduce basic construct of Verilog and comparison with VHDL.

SYLLABUS

Introduction to Hardware Design: Digital System Design Process, Hardware Description Languages, Hardware Simulation, Hardware Synthesis, Levels of Abstraction.

VHDL Background: VHDL History, Existing Languages, VHDL Requirements, The VHDL Language.

Design Methodology Based on VHDL: Elements of VHDL, Top down Design, Top down Design with VHDL, Subprograms, VHDL Operators, Conventions and Syntax.

Basic Concepts in VHDL: Characterizing Hardware Languages, Objects and Classes, Signal Assignments, Concurrent and Sequential Assignments.

Design Organization: Definition and Usage of Subprograms, Packaging Parts and Utilities, Generic and configuration, Design Configuration and Libraries.

Utilities for High-Level Descriptions: Type Declarations, VHDL Operators, Subprogram Parameter Types and Overloading, Predefined Attributes, User Defined Attributes.

Behavioral Description of Hardware: Process Statement, Assertion Statement, Sequential Wait Statements.

Introduction to Verilog: Overview of Digital design with Verilog HDL, basic concepts, Instances, Component of a simulation, modules & Ports, System Task and complier directives

Various types of modeling in Verilog: Introduction Gate level modeling, Behavioral Modeling, Modeling of various combinational and sequential circuits using Verilog.

COURSE OUTCOME

At the end of the course the students shall be able to:

1. Understand about the Design Steps with VHDL
2. Understand main programming technique with VHDL
3. Learn simulation techniques and test bench creation
4. Understand how to Design a simple digital circuit Using VHDL
5. Understand the basic concepts of Verilog

TEXT BOOKS:

1. J. Bhasker, *A VHDL Primer*, Third Edition, PH/Pearson, 1999.
2. J. Bhasker, *A VHDL Synthesis Primer*, Second Edition, Star Galaxy, 1998.
3. J. Bhasker, *A Verilog HDL Primer*, Second Edition, Star Galaxy, 1999.
4. J. Bhasker, *A Verilog Synthesis : A Practical Primer*, Star Galaxy, 1998.
5. M. J. S. Smith, *Application Specific Integrated Circuits*, AW/Pearson, 1997.

REFERENCE BOOKS:

1. Z. Navabi, *VHDL : Analysis and Modeling of Digital Systems,* Second Edition, MH, 1998.

2. J. Armstrong and F. G. Gray, *VHDL Design Representation and Synthesis*, Second Edition, PH/Pearson, 2000.

3. P. J. Ashenden, *The Designer's Guide to VHDL*, Second Edition, Morgan Kaufmann, 2001.

4. D. Naylor and S. Jones, *VHDL : A Logic Synthesis Approach*, Chapman & Hall, 1997.

5. C. H. Roth, *Digital System Design with VHDL*, PWS/Brookscole, 1998.

6. M. G. Arnold, *Verilog Digital Computer Design : Algorithms to Hardware*, PH, 1999.

7. Z. Navabi, *Verilog Digital System Design*, MH, 1999.

8. S. Palnitkar, *Verilog HDL : A Guide to Digital Design and Synthesis*, PH/Pearson, 1996.

9. K. Coffman, *Real World FPGA Design with Verilog*, PH, 2000.
10. D. R. Smith and P. D. Franzon, *Verilog Styles for Synthesis of Digital Systems*, AW/Pearson, 2001.
11. S. M. Trimberger, *FPGA Technology*, Kluwer, 1992.
12. J. V. Oldfield and R. C. Dorf, *FPGAs : Reconfigurable Logic for Rapid Prototyping and Implementation of Digital Systems*, Wiley, 1995.
13. R. C. Seals and G. F. Whapshott, *Programmable Logic : PLDs and FPGAs*, MH, 1998.

E16V-607 EMBEDDED SYSTEM DESIGN -I

L T P CR			
4 0 0 4	**Theory**	**:**	**75**
	Class Work	**:**	**25**
	Total	**:**	**100**
	Duration of Exam	**:**	**3 Hrs.**

Course Objective:

1. To introduce students about 8051 microcontroller, architecture & programming model.
2. To introduce the students about instruction set of 8051 addressing models & assembly language programming.
3. To introduce the students about timer & serial communication.
4. To introduce the students about interrupt programming and interfacing LCD, sensors & stepper motors with 8051 microcontroller.
5. To introduce the students about the interfacing of ADC/ DAC, external memory and 8255with 8051 microcontroller.
6. To introduce the students about 68HC11 microcontroller, its architecture, instruction set & programming model and its interfacing with peripherals.
7. To introduce the students to real time operating system.

SYLLABUS

MICROCONTROLLER 8051

Introduction, 8051 architecture and programming model. Internal RAM and registers, I/O ports, Interrupt system

PROGRAMMING WITH 8051

Jump, Loop and Call instructions, I/O port programming, Addressing modes, Arithmetic Instructions and programs Logic Instructions and programs, Single bit Instructions. Assembly Language Programming, Programming in C Language.

PERIPHERALS & INTERFACING

Timers and counters Serial Communications, Interrupts programming, Interfacing LCD, ADC and sensors, Interfacing stepper motors, keyboards and DAC‟S.Interfacing external memory and 8255

MOTOROLA 68HC11 MICROCONTROLLER

Instructions and addressing modes – operating modes – Hardware reset, Interrupt system, Parallel I/O ports – Flats – Real time clock – Programmable timer – pulse accumulator, Serial communication interface – A/D converter – hardware expansion – Basic Assembly Language programming.

REAL TIME OPERATING SYSTEM

Real time operating system overview, Exposure to Windows CE, QNX, Micro kernels and pc/US of introduction to process models. Interrupt routines in an RTOS environment. Encapsulation semaphores and queues, hard real-time scheduling considerations, saving memory space.

COURSE OUTCOME

Course Outcomes:

On successful complete of this course, the students should be able to:

1. Understand the architecture, interrupt system & instruction set of 8051 microcontroller and to understand the addressing modes & write the assemble language program of 8051 microcontroller.
2. Understand the interfacing the techniques with 8051microcontroller. To interface A/D converter, D/A converter, external memory & 8255.
3. Understand the architecture, instruction set and interrupt system of 68HC11 microcontroller. To interface I/O devices, A/D converter, D/A converter & memory with 68 HC 11.
4. Understand the real time operating system.

TEXT BOOKS

1. Kenneth Ayala “The 8051 Micro controller Architecture, programming and Application” Penram Publication

2. M.A. Mazizi & J.G. Mazidi, The 8051 Micro controller:, Pearson Education

3. Gene. H.Miller, “Micro Computer Engineering”, Pearson Education, 2003.

4. Rajkamal , “Embedded System Design” Tata McGrawHill

E16V-609 EMBEDDED SYSTEM LAB -I

L T P CR			
0 0 2 1	**External**	**:**	**35**
	Internal	**:**	**15**
	Total	**:**	**50**
	Duration of Exam	**:**	**3 Hrs.**

List of Experiments:

1. To generate 10 KHz square wave.
2. To generate 10 KHz square wave on providing an Interrupt INT1.
3. To perform serial communication between two kits.
4. Temperature Measurement Interface (ET-Temp).
5. Pressure Measurement Interface (ET-Pressure).
6. Speed Control of DC Motor using PWM.
7. AC voltage regulation using PWM.

Course Outcomes: On successful completion of this course, the students should be able to:

- Generate square wave of given period using 8051 microcontroller.
- Interface peripherals to 8051 microcontroller.
- Write experimental reports and work in a team in professional way.

E16V-611 DIGITAL VLSI DESIGN LAB

L T P CR			
2 0 0 1	**External**	**:**	**35**
	Internal	**:**	**15**
	Total	**:**	**50**
	Duration of Exam	**:**	**3 Hrs.**

List of Experiments:

1. To study the Tanner Tools-S-edit, T-spice, W-edit & L-edit.
2. To study & analyse the DC behaviour of CMOS inverter.
3. To study & analyse the transient behaviour of the CMOS inverter.
4. To perform the AC analysis of a CMOS Inverter.
5. To Design & Simulate CMOS NAND gate & CMOS NOR gate.
6. To Design & Simulate 2:1 MUX.
7. To Design & Simulate CMOS Half adder & CMOS Full Adder.
8. To Design & Simulate CMOS one bit Comparator using gates.
9. To Design & Simulate CMOS Even/Odd Parity Generator.
10. To draw the Layout of a CMOS inverter using L-edit & Simulate it.

Course Outcomes: On successful completion of this course, the students should be able:

- To design logic circuit using CMOS and NMOS technology in S-Edit.
- To study VTC characteristics and current- voltage characteristics of NMOS and CMOS circuits.
- To simulate the given logic circuit and study its DC, AC and transient behaviour using T-SPICE and W-Edit.
- To draw layout in L-Edit.
- Write experimental reports and work in a team in professional way.

E16V-613 **HDL LAB**

L T P CR			
0 0 2 1	**External**	**:**	**35**
	Internal	**:**	**15**
	Total	**:**	**50**
	Duration of Exam	**:**	**3 Hrs.**

List of Experiments:

1. To design all gates using VHDL.
2. Write VHDL programs for the following circuits, check the wave forms and the hardware generated
   a. half adder b. full adder
3. Write VHDL programs for the following circuits, check the wave forms and the hardware generated
   a. multiplexer b. demultiplexer
4. Write VHDL programs for the following circuits, check the wave forms and the hardware generated
   a. decoder b. encoder
5. Write a VHDL program for a comparator and check the wave forms and the hardware generated
6. 6 Write a VHDL program for a code converter and check the wave forms and the hardware generated.
7. Write a VHDL program for a FLIP-FLOP and check the wave forms and the hardware generated
8. Write a VHDL program for a up/down counter and check the wave forms and the hardware generated
9. Write a VHDL program for a mod-n counter and check the wave forms and the hardware generated
10. Write VHDL programs for the following circuits check the wave forms and the hardware generated
    a. Storage register b. Shift register
11. Write a VHDL program for ALU of microcomputer and check the wave forms and the hardware generated.
12. Write a Verilog program to implement half/full adder and check the waveform generated.
13. Write verilog programs for the following circuits, check the wave forms and

the hardware generated

a. multiplexer b. demultiplexer c. encoder d. decoder

14. Write a Verilog program for a FLIP-FLOP and check the wave forms and the hardware generated.
15. To implement any three (given above) on FPGA/CPLD kit.

Course Outcomes: On successful completion of this course, the students should be able to:

- Develop VHDL code for basic gates.
- Create VHDL code for various combinational circuits using different statements.
- Create VHDL code for various sequential circuits using different statements.
- Develop VHDL code for ALU of microcomputer.
- Implement basic gates, combinational circuits & sequential circuits on FPGA/CPLD kit.
- Write experimental reports and work in a team in professional way.

E16V--602 **ANALOG VLSI DESIGN**

L T P CR			
4 0 0 4	**Theory**	**:**	**75**
	Class Work	**:**	**25**
	Total	**:**	**100**
	Duration of Exam	**:**	**3 Hrs.**

COURSE OBJECTIVE

1. To learn about MOS/BJT analog processing.
2. To learn about the designing of single stage amplifiers.
3. To learn about the multistage amplifiers design parameters.
4. To learn about the current mirrors
5. To learn about the operational amplifiers designing procedure.
6. To learn about the A to D converters.
7. To learn about the switched capacitors circuits

SYLLABUS

Small Signal & large signal Models of MOS & BJT transistor. Analog MOS Process

MOS & BJT Transistor Amplifiers : Single transistor Amplifiers stages: Common Emitter, Common base, Common Collector, Common Drain, Common Gate & Common Source Amplifiers

Multiple Transistor Amplifier stages: CC-CE, CC-CC, & Darlington configuration, Cascode configuration, Differential Amplifiers: Differential pair & DC transfer characteristics.

Current Mirrors, Active Loads & References

Current Mirrors: Simple current mirror, Cascode current mirrors, Widlar current mirror, Wilson Current mirror, etc. Active loads, Voltage & current references. Analysis of Differential Amplifier with active load, supply and temperature independent biasing techniques, Frequency Response.

Operational Amplifier: Applications of operational Amplifier, theory and Design; Definition of Performance Characteristics; Design of two stage MOS Operational Amplifier, two stage MOS operational Amplifier with cascodes, MOS telescopic-cascode operational amplifiers, MOS Folded-cascode operational amplifiers, Frequency response & compensation.

Nonlinear Analog Circuits:

Digital-to-Analog (D/A) and Analog-to-Digital (A/D) Converters, Voltage controlled oscillator, Comparators, Phase Locked Loops (PLL)

OTA & Switched Capacitor filters

OTA Amplifiers. Switched Capacitor Circuits and Switched Capacitor Filters.

COURSE OUTCOME

1. Student will be able learn about analog signal processing through MOS/BJT devices.
2. Student will be able to identify the design procedure of single stage and multistage amplifier for for analog octagon design with minimum power and area.
3. Student will be able to investigate/identify about the analog octagon design parameters for any design.
4. Students can design the multi bit analog to digital converters with variable performances and switched capacitor circuits (as per the requirement/ with latest technology nodes).
5. Understanding the design process of current mirrors and OPAMP circuits.

TEXT BOOKS

1. Paul B Gray and Robert G Meyer, "Analysis and Design of Analog Integrated Circuits".
2. R Gregorian and G C Temes, Analog MOS Integrated Circuits for Signal Processing, John Wiley, 1986.
3. Allen and Holberg , "CMOS Analog Circuit Design" oxford University Press

References:

1. D. A. Johns and Martin, Analog Integrated Circuit Design, John Wiley, 1997.
2. R Gregorian and G C Temes, Analog MOS Integrated Circuits for Signal Processing, John Wiley, 1986.
3. Behzad Razavi, "Principles of data conversion system design", S.Chand and company Ltd, 2000. John Wiley
4. Kenneth R. Laker, Willy M.C. Sensen, " Design of Analog Integrated circuits and systems", McGraw Hill, 1994.

E16V-604 IC FABRICATION TECHNOLOGY

L T P CR			
4 0 0 4	**Theory**	**:**	**75**
	Class Work	**:**	**25**
	Total	**:**	**100**
	Duration of Exam	**:**	**3 Hrs.**

COURSE OBJECTIVE

1. To study Clean room and safety requirements, Wafer cleaning processes and wet chemical etching techniques.
2. To learn Solid State diffusion modelling and technology,Ion Implantation modelling, technology and damage annealing.
3. To study Kinetics of Silicon dioxide growth both for thick, thin and ultrathin films. Oxidation technologies in VLSI and ULSI.
4. To study Photolithography, E-beam lithography and newer lithography techniques for VLSI/ULSI.
5. To learn CVD techniques for deposition of polysilicon, silicon dioxide, silicon nitride and metal films, Epitaxial growth of silicon.
6. To study Evaporation and sputtering techniques, Failure mechanisms in metal interconnects,Multi-level metallisation schemes.

SYLLABUS

Environment for VLSI Technology : Clean room and safety requirements. Wafer cleaning processes and wet chemical etching techniques.

Impurity incorporation: Solid State diffusion modelling and technology; Ion Implantation modelling, technology and damage annealing; characterisation of Impurity profiles.

Oxidation : Kinetics of Silicon dioxide growth both for thick, thin and ultrathin films. Oxidation technologies in VLSI and ULSI; Characterisation of oxide films; High k and low k dielectrics for ULSI.

Lithography : Photolithography, E-beam lithography and newer lithography techniques for VLSI/ULSI; Mask generation.

Chemical Vapour Deposition techniques : CVD techniques for deposition of and polysilicon, silicon dioxide, silicon nitride metal films; Epitaxial growth of silicon; modelling and technology.

Metal film deposition : Evaporation and sputtering techniques. Failure mechanisms in metal interconnects; Multi-level metallisation schemes.

Plasma and Rapid Thermal Processing: PECVD, Plasma etching and RIE techniques; RTP techniques for annealing, growth and deposition of various films for use in ULSI.

Recent Trends in Fabrication, Process integration for NMOS, CMOS and Bipolar circuits; Advanced MOS technology.

COURSE OUTCOME

At the end of the course the students shall be able to:

- Understand the environment conditions for VLSI technology and study of various etching techniques.
- Understand the modeling for solid state diffusion, ion implantation and oxidation technology in VLSI.
- Understand various lithographic, processes, and CVD techniques.
- Understand the metal film deposition and rapid thermal processing.
- Understand the process integration to MOS and bipolar circuits.

TEXT BOOKS

1. S.K. Ghandhi, VLSI Fabrication Principles, John Wiley Inc., New York, 1994(2nd Edition).
2. S.M. Sze (Ed), VLSI Technology, 2nd Edition, McGraw Hill, 1988.
3. Plummer, Deal , Griffin “Silicon VLSI Technology: Fundamentals, Practice & Modeling” PH, 2001.
4. P. VanZant , “Microchip Fabrication”, 5th Edition, MH , 2000.

E16V-606 EMBEDDED SYSTEM DESIGN-II

L T P CR			
4 0 0 4	**Theory**	**:**	**75**
	Class Work	**:**	**25**
	Total	**:**	**100**
	Duration of Exam	**:**	**3 Hrs.**

COURSE OBJECTIVES:

- To introduce the students about PIC Microcontroller Architecture
- To introduce the students about PIC Hardware
- To introduce the students about Programming with PIC
- To introduce the students about Hardware Interfacing
- To introduce the students about ARM Processor Fundamentals

SYLLABUS

THE PIC MICROCONTROLLER ARCHITECTURE
CPU, ALU , Data Movement, The Program Counter and Stack, Reset , Interrupts, Architecture Differences, Mid-Range instruction Set

PIC HARDWARE FEATURES
Power Input and Decoupling , Reset, Watchdog Timer, System Clock/Oscillators, Configuration Registers, Sleep , Hardware and File Registers, Parallel Input Output, Interrupts, Prescaler , The OPTION Register , Mid-Range Built-In EEPROM Flash Access, TMR1 andTMR2 Serial I/0, Analog I/0, Parallel Slave Port (PSP), External Memory Connections , In-Circuit Serial Programming (ISCP)

PROGRAMMING WITH PIC
Assembly Language Programming, Hex File Format, Code-Protect Features, Programming, PIC Emulators

HARDWARE INTERFACING
Estimating Application Power Requirements, Reset, lnterfacing to External Devices, LEDs, Switch Bounce , Matrix Keypads , LCDs, Analog I/O, Relays and Solenoids, DC and Stepper Motors, Servo Control Serial Interfaces

ARM PROCESSOR FUNDAMENTALS
Registers, State and Instruction Sets, Pipeline, Memory Management, Introduction to the ARM Instruction Set

COURSE OUTCOME

- Understand about PIC Microcontroller Architecture
- Understand about PIC Hardware
- Understand about Programming with PIC
- Understand about Hardware Interfacing
- Understand about ARM Processor Fundamentals

TEXT BOOKS

1. Programming and customizing PIC microcontroller- Myke Predko, Mc- Graw Hill.
2. John.B. Peatman, “Design with PIC Micro controller”, Pearson Education, 2003.
3. Steave Furber, “ARM system – on – chip architecture” Addison Wesley, 2000.

E16V-608A ASICs and FPGA

L T P CR			
4 0 0 4	**Theory**	**:**	**75**
	Class Work	**:**	**25**
	Total	**:**	**100**
	Duration of Exam	**:**	**3 Hrs.**

COURSE OBJECTIVES

- To study the concept of ASICs & FPGAs, logistics of ASICs, FPGAs and its economics
- To study the hardware description languages, Logic design Review, Behaviour, dataflow, structural modeling, control statements, FSM modeling
- To study the CMOS structure, Classical, CMOS (Deep Sub-micron), ASIC Methodologies
- To study the fabrication of MOSFET, Design methodologies, design for testability.
- To study the concept of FPGA, Programmable logic FPGA, Configuration logic blocks, Function Generator, ROM implementation, RAM implementation, time skew buffers, FPGA Design tools, Network-on-chip, Adaptive System-on-chip, AES ASIC Implementation, Advanced FPGA Design
- To study the logic synthesis, Fundamentals, logic synthesis with synopsis, physical design compilation, simulation, implementation. Floor planning and placement, Commercial EDA tools for synthesis.
- To study the concept of testing, Advanced interconnects and testing techniques

SYLLABUS

Introduction: course outline, logistics introduction to ASICs, FPGAs, economics

HDL: Logic design Review, Behavior, dataflow, structural modeling, control statements, FSM modeling

CMOS Review: Classical, CMOS (Deep Sub-micron), ASIC Methodologies

Fabrication of MOSFET: MOS Transistor, Design methodologies, design for testability.

FPGA: Programmable logic FPGA, Configuration logic blocks, Function Generator, ROM implementation, RAM implementation, time skew buffers, FPGA Design tools, Network-on-chip, Adaptive System-on-chip, AES ASIC Implementation, Advanced FPGA Design

Logic synthesis: Fundamentals, logic synthesis with synopsis, physical design compilation, simulation, implementation. V Floor planning and placement, Commercial EDA tools for synthesis.

Testing: Advanced interconnects and testing techniques

COURSE OUTCOME

At the end of the course the students shall be able to:

- Understand the concept of Application specific & field programmable integrated circuits. Understand the concept of FPGA, implementation of various digital circuits using FPGA, FPGA design flow.
- Understand the HDL & design of various digital circuits using different style of modeling.
- Understand the concept of CMOS, its current voltage characteristics & various ASIC methodologies. Design of various types of MOSFETs using different fabrication techniques.
- Understand the circuit partitioning, floor planning and placement algorithms & use of these algorithms to design an IC.
- Understand the concept of testing, various techniques and interconnects

TEXT BOOKS

1. Bushnell and Agarwal “Essentials of Electronic Testing” KLUWER Academic Publishers.

E16V-608B CAD SYSTEM ENVIRONMENT

L T P CR			
4 0 0 4	**Theory**	**:**	**75**
	Class Work	**:**	**25**
	Total	**:**	**100**
	Duration of Exam	**:**	**3 Hrs.**

Course Objectives:

- To introduce the students about the basic concepts of Operating System
- To introduce the students about the commands of Unix and Linux
- To introduce the students about SUN OS and Windows NT,XP Environment
- To make the students familiar with PVM

SYLLABUS

Basic Concept of Operating System: Evolution of operating system, fundamental of operating system functions, multiprogramming, multiprocessing, time sharing systems and real time systems.

Linux : Brief History , Linux Distributions , Using the Emacs Editor , Using the vi Editor , Using the Pico Editor , Introduction to Users and Groups Essentials of Effective User, Group, and Password Management , Introduction to the Linux Kernel ,Using Kernel Modules ,Compiling the Linux Kernel ,Installing the Linux Kernel . File System , Disk Geometry

UNIX: Familiarity with different shells, UNIX Utilities like tar, make, yacc, lex, lint, debugger etc. Programming Tools: Perl, tcl/ tk File formats .tgz, .tar, X-term environment

SUN OS: The Solaris Operating Environment, Specific Features, Solaris Web Start Wizards, DHCP, Web-based enterprise management, Solaris Management Console, role-based access control (RBAC), Sun Management Center, Solaris Volume Manager, Solaris Resource Manager, Solaris Bandwidth Manager, Extensive Linux Compatibility

Windows NT, Win 8/10 Environment

Familiarity with PVM: creating a parallel virtual environment, initiating server and daemons, PVM library routines, XPVM

Course Outcomes: At the end of the course the students shall be able to:

- Understand the basic concepts of Operating System and apply the programming skills for real time systems.
- Understand the commands of Unix and Linux
- Understand about SUN OS and Windows NT,XP Environment
- Familiarization with PVM, XPVM library routine tool and parallel internal environment.

E16V-608C **CAD for VLSI**

L T P CR			
4 0 0 4	**Theory**	**:**	**75**
	Class Work	**:**	**25**
	Total	**:**	**100**
	Duration of Exam	**:**	**3 Hrs.**

Course Objectives:

- To introduce the students about VLSI design methodologies and supporting CAD environment
- To introduce the students about Schematic editors, Layout Analysis and Simulation
- To introduce the students about testing ICs and fault diagnosis
- To introduce the students about PLA testing and Memory testing
- To introduce the students about recent topics in CAD-VLSI

Syllabus

Introduction to VLSI design methodologies and supporting CAD environment.

Schematic editors: Parsing: Reading files, describing data formats, Graphics & Plotting Layout. Layout Editor: Turning plotter into an editor. Layout language: Parameterized cells, PLA generators, Introduction to Silicon compiler, Datapath. Compiler, Placement & routing, Floor planning.

Layout Analysis: Design rules, Object based DRC, Edge based layout operations. Module generators.

Simulation: Types of simulation, Behavioral simulator, logic simulator, functional simulator & Circuit simulator.

Simulation Algorithms: Compiled code and Event-driven. Optimization Algorithms: Greedy methods, simulated annealing, genetic algorithm and neural models.

Testing ICs: Fault simulation, Aids for test generation and testing. Computational complexity issues: Big Oh and big omega terms.

Recent topics in CAD-VLSI: Array compilers, hardware software co-design, high-level synthesis tools and VHDL modeling.

Course Outcomes: At the end of the course the students shall be able to:

- Understand about VLSI design methodologies and supporting CAD environment
- Understand about Schematic editors, Layout Analysis and Simulation on functional
- Testing ICs and fault diagnosis with computational uses.

- Understand about PLA testing and Memory testing and get familiar with high level synthesis tool & VHDL modeling.

TEXT BOOKS

1. Trimburger," Introduction to CAD for VLSI", Kluwer Academic publisher, 2002

2. Naveed Shervani, "Algorithms for VLSI physical design Automation", Kluwer Academic Publisher, Second edition.

E16V 610 **ANALOG VLSI LAB**

L T P CR			
0 0 2 1	**External**	**:**	**35**
	Internal	**:**	**15**
	Total	**:**	**50**
	Duration of Exam	**:**	**3 Hrs.**

1. (A) Design and simulate the characteristics of NMOS for different value of Vgs & Vds . Calculate current for unit size device at 180nm technology.

   (B) Design and simulate the transconductance of device with overdrive signal and aspect ratio of the device. Plot the transfer characteristics of NMOS . Repeat exercise for PMOS device.
2. Design and simulate the parasitic components of NMOS and PMOS for 180nm technology node &validation of mathematical and simulation result when device is operating in different regions.
3. Design and simulate the performance of common source configuration with resistive load and diode connected load. Find out various parameters: (a)Input and Output resistance (b)Gain using transient and DC analysis. Verify analytical versus simulation.
4. Design and simulate the performance of common source amplifier, for bandwidth using 180nm technology node and how it can be further improved. Explain in detail and also find its output resistance.
5. Design and simulate the characteristics of various current mirrors (Basic , Wilson, Improved , Cascode) using 180nm technology. And calculate the output resistance for each.
6. Design and simulate the switching times of various logic gates for 180nm , 130nm and 100nm technology node.
7. Deign and simulate the characteristics of differential amplifier with different nodes.
8. Design and simulate and validate the mathematical model for gain , input and output impedance for Push –Pull amplifier.

Course Outcomes: On successful completion of this course, the students should be able to:

- Design and simulate NMOS, PMOS and CMOS at 180nm, 130nm and 100 nm technology.
- Design and simulate various amplifiers (CS, differential, push-pull, etc) using CMOS technology .

- Find various parameters like power consumption, delay, input and output resistance of the given logic circuit.
- Simulate various current mirror circuits using 180nm technology.

E16V 612 **Embedded System Lab –II**

L T P CR			
0 0 2 1	**External**	**:**	**35**
	Internal	**:**	**15**
	Total	**:**	**50**
	Duration of Exam	**:**	**3 Hrs.**

1. Write a program to add two 8 bit numbers using direct addressing mode.
2. Write a program to add two 8 bit numbers using indirect addressing mode.
3. Write a program to subtract two 8 bit numbers using direct and indirect addressing mode.
4. Write a program to find 1's complement of a number using PIC microcontroller.
5. Write a program to find 2's complement of a number using PIC microcontroller.
6. Write a program to move a block of data using PIC.
7. Write a program to multiply two numbers.
8. Write a program to divide two numbers.
9. Write a program to generate a square wave.
10. Write a program to generate 2 sec delay using PIC.

Course Outcomes: On successful completion of this course, the students should be able :

- To perform basic operations (addition, subtraction, multiplication and division) on two numbers using PIC microcontroller.
- To find 1's and 2's complement of a number using PIC microcontroller.
- To generate delay using PIC microcontroller.
- To move a block of data using PIC microcontroller.

E16V-701 ADVANCED DIGITAL SIGNAL PROCESSING

L T P CR			
4 0 0 4	**Theory**	**:**	**75**
	Class Work	**:**	**25**
	Total	**:**	**100**
	Duration of Exam	**:**	**3 Hrs.**

COURSE OBJECTIVES

1. To analyze of different type of signals and systems.
2. To analyze the DFFT and DFT and their properties, fast fourier transform (FFT), decimation in time algorithm, decimation in frequency algorithm.
3. To understand the use of sampling and reconstruction. To understand the use of z-transform in discrete time systems.
4. To analyze the different types of structures of FIR and IIR systems. To design IIR filters, design of FIR using windows, properties of FIR filters.
5. To Describe the effects of finite word lengths and truncation and rounding in digital signal processing for IIR and FIR filters.

SYLLABUS

1. Introduction of DSP: Introduction to Signal Processing, Discrete Linear Systems, superposition Principle, Unit-Sample response, stability & causality Criterion.

2. Fourier Transform & inverse Fourier transform: Frequency domain design of digital filters, Fourier transform, use of Fourier transform in Signal processing. The inverse fourier transform, Sampling continuous function to generate a sequence, Reconstruction of continuous -time signals from Discrete-time sequences.

3. DFT & FFT & Z transform with Applications: Discrete Fourier transform, properties of DFT, Circular Convolution, Fast Fourier Transform, Realizations of OFT. The Ztransform, the system function of a digital filter, Digital Filter implementation from the system function, the inverse Z- transform, properties & applications, Special computation of finite sequences, sequence of infinite length & continuous time signals, computation of fourier series & time sequences from spectra.

4. Digital Filter Structure & Implementation: Linearity, time- invariance & causality, the discrete convolution, the transfer function, stability tests, steady state response, Amplitude & Phase characteristics, stabilization procedure, Ideal LP Filter, Physical reliability & specifications.FIR Filters, Truncation windowing & Delays, design example, IIR Filters: Review of design of analog filters & analog frequency transformation. Digital frequency transformation. Design of LP filters using impulse invariance method, Bilinear transformation, Phase equalizer, digital all pass filters.

5. Implementation of Filters: Realization block diagrams, Cascade & parallel realization, effect of infinite-word length, transfer function of degree 1&2, Sensitivity

comparisons, effects of finite precision arithmetic on Digital filters.

COURSE OUTCOMES:

At the end of the course the students will be able to:

- Analyze of different type of signals and systems.
- Analyze the DTFT and DFT and their properties, fast fourier transform (FFT), decimation in time algorithm, decimation in frequency algorithm.
- Understand the use of sampling and reconstruction. Understand the use of z-transform in discrete time systems.
- Analyze the different types of structures of FIR and IIR systems. Design IIR filters, design of FIR using windows, properties of FIR filters.
- Describe the effects of finite word lengths and truncation and rounding in digital signal processing for IIR and FIR filters

TEXT BOOKS

1 Alam V. Oppenheim & Ronald W. Schafer, "Digital Signal Processing" HI. 2 JG Proakis, "Digital Signal Processing", (PHI) 3rd Edition.

REFERENCE BOOKS

I. Rabiner & Gold, "Theory & application of digital Signal Processing", PHI 1992. 2. Roman kuc, "Introduction to Digital Signal Processing," McGraw hill Edition.

E16V-703 **NANOTECHNOLOGY**

L T P CR			
4 0 0 4	**Theory**	**:**	**75**
	Class Work	**:**	**25**
	Total	**:**	**100**
	Duration of Exam	**:**	**3 Hrs.**

COURSE OBJECTIVE

1. To learn basic crystallography, Crystals and their imperfections, Diffusion, Nucleation and crystallization, Phase transformations.
2. To study various physical properties of materials, Density of states, Coulomb blockade, Kondo effect, Quantum Hall Effect.
3. To study various types of Nanostructures, Properties of Nanomaterials, applications of Nano structures.
4. To learn the Characterization of Nanomaterials.

SYLLABUS

Unit - I Atomic structure

Basic crystallography, Crystals and their imperfections, Diffusion, Nucleation and crystallization, Metals, Semiconductors and Insulators, Phase transformations, Ceramic materials.

Unit – II Physical Properties of Materials

Electrical and Thermal properties, Optical properties of materials, Magnetic properties of materials, Density of states, Coulomb blockade, Kondo effect, Hall effect, Quantum Hall Effect.

Unit – III Nanostructures

Introduction to Nanotechnology, Zero dimensional nanostructures – Nano particles, One dimensional nanostructures – Nano wires and Nano rods, Two dimensional nanostructures – Films, Special nano materials, Nano structures fabricated by Physical Techniques, Properties of Nanomaterials, Applications of Nano structures, Basics of Nano Electronics.

Unit – IV Characterization of Nanomaterials

SPM Techniques – Scanning Tunneling Microscopy, Atomic Force Microscopy, Magnetic Force Microscopy, Electron Microscopy – Scanning Electron Microscope, Transmission Electron Microscope

COURSE OUTCOMES

At the end of the course the students shall be able to:

1. Understand atomic structure, diffusion, nucleation and crystallization of materials.
2. Understand the physical properties of materials, coulomb blockade and hall effect.
3. Understand the fundamental of nanostructures and nanoelectronics
4. Understand the fundamental of various characterization techniques like STM, SEM, TEM and AFM.

TEXT BOOKS/ REFERENCE BOOKS ;

1.Introduction to solid state Physics: C.Kittel
2. Introduction to theory of solids: H.M. Roenberg
3. Physics and Chemistry of materials: Joel I. Gersten
4.Handbook of Nanotechnology: Bharat Bhushan(springer)

E16V-705A **VLSI ARCHITECTURES**

L T P CR			
4 0 0 4	**Theory**	**:**	**75**
	Class Work	**:**	**25**
	Total	**:**	**100**
	Duration of Exam	**:**	**3 Hrs.**

Course Objectives:

- To introduce the students about parallel computer models
- To introduce the students about Program and network properties
- To introduce the students about System Interconnect Architectures
- To introduce the students about Advanced processors and Pipelining
- To introduce the students about Memory Hierarchy Design
- To introduce the students about Multiprocessor architectures and Scalable point – point interfaces

SYLLABUS

Parallel computer models:
The state of computing, Classification of parallel computers, Multiprocessors and multicomputers, Multivector and SIMD computers.

Program and network properties:
Conditions of parallelism, Data and resource Dependences, Hardware and software parallelism, Program partitioning and scheduling, Grain Size and latency, Program flow mechanisms, Control flow versus data flow, Data flow Architecture, Demand driven mechanisms, Comparisons of flow mechanisms

System Interconnect Architectures:
Network properties and routing, Static interconnection Networks, Dynamic interconnection Networks, Multiprocessor system Interconnects, Hierarchical bus systems, Crossbar switch and multiport memory, Multistage and combining network.

Advanced processors:
Advanced processor technology, Instruction-set Architectures, CISC Scalar Processors, RISC Scalar Processors, Superscalar Processors, VLIW Architectures, Vector and Symbolic processors

Pipelining:
Linear pipeline processor, nonlinear pipeline processor, Instruction pipeline Design, Mechanisms for instruction pipelining, Dynamic instruction scheduling, Branch Handling techniques, branch prediction, Arithmetic Pipeline Design, Computer arithmetic principles, Static Arithmetic pipeline, Multifunctional arithmetic pipelines

Multiprocessor architectures:
Symmetric shared memory architectures, distributed shared memory architectures, models of memory consistency, cache coherence protocols (MSI, MESI, MOESI),

scalable cache coherence, overview of directory based approaches, design challenges of directory protocols, memory based directory protocols, cache based directory protocols, protocol design tradeoffs, synchronization,

Reconfigurable Computing: Motivation, architectures, static and dynamic reconfiguration, reconfiguration costs and models, building blocks of programmable logic devices. Computational models of reconfigurable computing systems.

1.Kai Hwang, "Advanced computer architecture"; TMH.
2.D. A. Patterson and J. L. Hennessey, "Computer organization and design," Morgan Kaufmann, 2nd Ed.

References:

1. J.P.Hayes, "computer Architecture and organization"; MGH.
2. Harvey G.Cragon,"Memory System and Pipelined processors"; Narosa Publication.
3. V.Rajaranam & C.S.R.Murthy, "Parallel computer"; PHI.
4. R.K.Ghose, Rajan Moona & Phalguni Gupta, "Foundation of Parallel Processing"; Narosa Publications.
5. Kai Hwang and Zu, "Scalable Parallel Computers Architecture"; MGH.
6. Stalling W, "Computer Organisation & Architecture";PHI.
7. D.Sima, T.Fountain, P.Kasuk, "Advanced Computer Architecture-A Design space Approach,"Addison Wesley,1997.
8. M.J Flynn, "Computer Architecture, Pipelined and Parallel Processor Design"; Narosa Publishing.

Course Outcomes: At the end of the course the students shall be able to:

- Understanding of a substantial body of knowledge of design methodologies and techniques applicable to VLSI technology.
- Application of knowledge together with a practical understanding of how efficiently various architectures function.
- Advance the knowledge and understanding of current developments in VLSI technology
- To introduce the key concepts of hardware/software communication to make trade-offs between the flexibility and the performance of a digital system.
- Students will gain design and implementation experience with case studies.

E16V-705B **EMBEDDED CONTROL SYSTEM**

L T P CR			
4 0 0 4	**Theory**	**:**	**75**
	Class Work	**:**	**25**
	Total	**:**	**100**
	Duration of Exam	**:**	**3 Hrs.**

Course Objectives:

- To introduce the students about Input Output Interfacing
- To introduce the students about design and interfacing of ADC and DAC
- To introduce the students about Asynchronous serial communication
- To introduce the students about interfacing of sensors and LCD
- To introduce the students about time-based measurements

SYLLABUS

INTRODUCTION

Controlling the hardware with software – Data lines, Address lines, Ports – Schematic representation – Bit masking – Programmable peripheral interface – Switch input detection – 74 LS 244

INPUT-OUTPUT DEVICES

Keyboard basics – Keyboard scanning algorithm – Multiplexed LED displays – Character LCD modules, LCD module display, Configuration – Time-of-day clock – Timer manager - Interrupts - Interrupt service routines, IRQ, ISR, Interrupt vector or dispatch table multiple-point - Interrupt-driven pulse width modulation.

D/A AND A/D CONVERSION

R 2R ladder - Resistor network analysis - Port offsets - Triangle waves analog vs. digital values - ADC0809 – Auto port detect - Recording and playing back voice - Capturing analog information in the timer interrupt service routine - Automatic, multiple channel analog to digital data acquisition.

ASYNCHRONOUS SERIAL COMMUNICATION

Asynchronous serial communication – RS-232, RS-485 – Sending and receiving data – Serial ports on PC – Low-level PC serial I/O module, Buffered serial I/O.

CASE STUDIES: EMBEDDED C PROGRAMMING

Multiple closure problems – Basic outputs with PPI – Controlling motors – Bi-directional control of motors – H bridge – Telephonic systems – Stepper control – Inventory control systems.

Course Outcomes: At the end of the course the students shall be able to:

- Understand about Input Output Interfacing

- Understand about design and interfacing of ADC and DAC
- Understand about Asynchronous serial communication
- Understand about interfacing of sensors and LCD
- Understand about time-based measurements

TEXT BOOKS:

1. Jean J. Labrosse, "Embedded Systems Building Blocks: Complete and Ready-To-Use Modules in C", The publisher, Paul Temme, 2003.
2. Ball S.R., „Embedded microprocessor Systems – Real World Design", Prentice Hall, 2001.

REFERENCE BOOKS:

1. Herma K, "Real Time Systems – Design for distributed Embedded Applications", Kluwer Academic, 2003.
2. Daniel W. Lewis, "Fundamentals of Embedded Software where C and Assembly meet", PHI, 2002.

E16V-705C **MIXED SIGNAL EMBEDDED SYSTEM**

L T P CR			
4 0 0 4	**Theory**	**:**	**75**
	Class Work	**:**	**25**
	Total	**:**	**100**
	Duration of Exam	**:**	**3 Hrs.**

Course Objectives:

- To introduce the students about System Design
- To introduce the students about design of ADC and DAC
- To introduce the students about PLL and its applications
- To introduce the students about interfacing of sensors and LCD
- To introduce the students about time-based measurements

SYLLABUS

INTRODUCTION TO SYSTEM DESIGN

Dynamic Range, Calibration, Bandwidth, Processor Throughput, Avoiding Excess Speed , Other System Considerations, Sample Rate and Aliasing

DAC & ADC

Introduction - Nyqusist rate converters – Over sampling converters - Pipelined/parallel converters - High speed ADC design, High speed DAC design and Mixed signal design for radar application - ADC and DAC modules used for LIGO.

PLL

Introduction - Frequency Synthesizers - Design of PLL and Frequency Synthesizers – PLL with voltage driven oscillator – PLL with current driven oscillator – ETPLL – PLL synthesizer oscillator by MC14046B

SENSOR INTERFACING

Sensors, Sensor Types , Amplifier Design , Interfacing of Temperature, Pressure, Displacement Transducer in Embedded System Environment

LCD AND INFRA RED

LCD Fundamentals, Response Time, Temperature Effects, Connection Methods, Different types of LCD Panels, Static Waveforms, Infra Red Detection and Transmission

TIME-BASED MEASUREMENTS

Measuring Period versus Frequency, Mixing, Voltage-to-Frequency Converters, Clock Resolution and Range, Extending Accuracy with Limited Resolution

Course Outcomes: At the end of the course the students shall be able to:

- To introduce the students about System Design
- To introduce the students about design of ADC and DAC

- To introduce the students about PLL and its applications
- To introduce the students about interfacing of sensors and LCD
- To introduce the students about time-based measurements

TEXT BOOKS:

1. Analog Interfacing to Embedded Microprocessors Real World Design, Stuart Ball.

2. Breems, "Continuous-Time Sigma Delta Modulations for A/D Conversion",. Kluwer, 2002.

REFERENCE BOOKS:

1. Allen, "CMOS Analog Circuit Design", Oxford, 2005.

2. Behzad Razavi, "Design of Analog CMOS integrated circuit", Tata McGraw Hill, 2004.

2. Michelle Steyaert, "Analog Circuit Design", Kluwer, 2003.

3. Gray & Meyer, Analysis and Design of Analog Integrated Circuits, Wiley, 2004.

4. Baker, CMOS Mixed-Signal Circuit Design, Wiley, 2004.

E16V-707A VLSI TESTING AND DESIGN FOR TESTABILITY

L T P CR			
4 0 0 4	**Theory**	**:**	**75**
	Class Work	**:**	**25**
	Total	**:**	**100**
	Duration of Exam	**:**	**3 Hrs.**

Course Objectives:

- To introduce the students about Physical defects and their modeling
- To introduce the students about Fault Simulation and Test Generation
- To introduce the students about Random, Exhaustive and Weighted Random Test Pattern Generations
- To introduce the students about PLA testing and Memory testing
- To introduce the students about Memory testing and Concept of Redundancy
- To introduce the students about recent trends in VLSI testing

SYLLABUS

Physical defects and their modeling; stuck at faults; Bridging Faults; Fault collapsing.

Fault Simulation: Deductive, Parallel and Concurrent; Critical Path Tracing.

Test Generation for Combinational Circuits: D-Algorithm, Boolean Difference, PODEM, and ATPG.

Random, Exhaustive and Weighted Random Test Pattern Generations, Aliasing and its effect on Fault coverage.

PLA Testing: cross-point Fault Model, Test Generation,

Memory testing: Permanent Intermittent and Pattern Sensitive Faults; Delay Faults and Hazards; Test Generation Techniques;

Test Generation for Sequential Circuits.

Scan Design. Scan path and LSSD, BILBO

Concept of Redundancy, spatial redundancy, Time redundancy

Recent trends in VLSI testing: Genetic Algorithms, Parallel Algorithms, Neural networks, nano scale testing

Course Outcomes: At the end of the course the students shall be able to:

- Understand physical defects and their modeling; stuck at faults; Bridging Faults; Fault

collapsing and fault Simulation: Deductive, Parallel and Concurrent and Critical Path Tracing.

- Understand Test Generation for Combinational Circuits: D-Algorithm, Boolean Difference, PODEM, and ATPG. Random, Exhaustive and Weighted Random Test Pattern Generations, Aliasing and its effect on Fault coverage.

- Understand PLA Testing: cross-point Fault Model, Test Generation, Memory testing: Permanent Intermittent and Pattern Sensitive Faults; Delay Faults and Hazards; Test Generation Techniques;

- Understand Test Generation for Sequential Circuit and Scan Design scan path and LSSD, BILBO.

- To understand concept of Redundancy, spatial redundancy, Time redundancy, recent trends in VLSI testing: Genetic Algorithms, Parallel Algorithms, Neural networks, nano scale testing

TEXT BOOKS

1. VLSI Testing: digital and mixed analogue digital techniques Stanley L. Hurst Pub:Inspec/IEE ,1999

E16V-707B **LOW POWER VLSI DESIGN**

L T P CR			
4 0 0 4	**Theory**	**:**	**75**
	Class Work	**:**	**25**
	Total	**:**	**100**
	Duration of Exam	**:**	**3 Hrs.**

Course Objectives:

- To learn about the need of low power designing
- To learn about the device scaling and leakage components
- To learn about SPICE simulation
- To learn about the leakage control at circuit level
- To learn about the Leakage control at the architecture level
- To learn about the clock distribution networks

Syllabus

Low power Basics

Need for low power VLSI chips, Sources of power dissipation on Digital Integrated circuits. Emerging Low power approaches. Physics of power dissipation in CMOS devices.

Device & Technology Impact on Low Power

Dynamic dissipation in CMOS, Transistor sizing & gate oxide thickness, Impact of technology Scaling, Technology & Device innovation.

Power estimation

Simulation Power analysis: SPICE circuit simulators, gate level logic simulation, capacitive power estimation, static state power, gate level capacitance estimation, architecture level analysis, data correlation analysis in DSP systems. .

Low Power Design

Circuit level: Power consumption in circuits. Flip Flops & Latches design, high capacitance nodes, low power digital cells library

Logic level: Gate reorganization, signal gating, logic encoding, state machine encoding, pre-computation logic

Low power Architecture & Systems: Power & performance management, switching activity reduction, parallel architecture with voltage reduction, flow graph transformation, low power arithmetic components, low power memory design.

Low power Clock Distribution: Power dissipation in clock distribution, single driver Vs distributed buffers, Zero skew Vs tolerable skew, chip & package co design of clock network

Algorithm & architectural level methodologies: Introduction, design flow, Algorithmic level analysis & optimization, Architectural level estimation & synthesis.

Course Outcomes: At the end of the course the students shall be able to:

- Understand of basics of MOS and need of low power design with modeling using SPICE CAD and cell based design and verification functionality, timing, power and power and parasitic effect in digital ICs.

- Understand of source of power dissipation in digital IC with system performance and reliability.

- Understand voltage scaling approaches with different design abstraction level and characterization of various power consumption models and clocking strategy.

- Understand of sequential circuits for low power, probalistic analysis BSIM and reduction techniques.

TEXT BOOKS

1. Gary K. Yeap, "Practical Low Power Digital VLSI Design", KAP, 2002

2. Rabaey, Pedram, "Low power design methodologies" Kluwer Academic, 1997

References:

1. Kaushik Roy, Sharat Prasad, "Low-Power CMOS VLSI Circuit Design" Wiley, 2000

E16V-707C ALGORITHM FOR VLSI DESIGN AUTOMATION

L T P CR			
4 0 0 4	**Theory**	**:**	**75**
	Class Work	**:**	**25**
	Total	**:**	**100**
	Duration of Exam	**:**	**3 Hrs.**

Course Objectives:

- To introduce the students about VLSI physical design automation and Fabrication
- To introduce the students about VLSI automation Algorithms
- To introduce the students about Floor planning & pin assignment
- To introduce the students about Global Routing and Detailed routing and compaction

Syllabus

VLSI physical design automation and Fabrication

VLSI Design cycle, New trends in VLSI design, Physical design cycle, Design style, Introduction to fabrication process, design rules, layout of basic devices

VLSI automation Algorithms:

Partitioning: problem formulation, classification of partitioning algorithms, Group migration algorithms, simulated annealing.

Floor planning & pin assignment: problem formulation, classification of floor planning algorithms, constraint based floor planning, floor planning algorithms for mixed block & cell design, chip planning, pin assignment, problem formulation, classification of pin assignment algorithms, General & channel pin assignment

Placement

Problem formulation, classification of placement algorithms, simulation base placement algorithms, recent trends in placement

Global Routing and Detailed routing: Problem formulation, classification of global routing algorithms, Maze routing algorithm, line probe algorithm, Steiner Tree based algorithms, performance driven routing

Detailed routing problem formulation, classification of routing algorithms, introduction to single layer routing algorithms, two layer channel routing algorithms, greedy channel routing, switchbox routing algorithms.

Over the cell routing & via minimization: two layers over the cell routers, constrained & unconstrained via minimization

Compaction: problem formulation, classification of compaction algorithms, one-dimensional compaction, two dimension based compaction, hierarchical compaction

Course Outcomes: At the end of the course the students shall be able to:

- Understand about VLSI physical design automation and Fabrication

- Understand about VLSI automation Algorithms
- Understand about Floor planning & pin assignment
- Understand about Global Routing and Detailed routing and compaction

TEXT BOOKS

1. Naveed Shervani, "Algorithms for VLSI physical design Automation", Kluwer Academic Publisher, Second edition.

REFERENCES

1. Christophn Meinel & Thorsten Theobold, "Algorithm and Data Structures for
2. VLSI Design", KAP, 2002Rolf Drechsheler : "Evolutionary Algorithm for VLSI", Second edition
3. Trimburger," Introduction to CAD for VLSI", Kluwer Academic publisher, 2002

E 711 V **ADSP Lab**

L T P CR			
0 0 2 1	**External**	**:**	**35**
	Internal	**:**	**15**
	Total	**:**	**50**
	Duration of Exam	**:**	**3 Hrs.**

1. To plot basic signal (Step, Impulse, Ramp, Exponential, Sine and Cosine signal) using MATLAB.
2. To find and plot convolution of to signals using MATLAB.
3. A) To generate frequency response of given system using MATAB.

   B) To study the frequency response of given function ($\frac{1+0.5s+0.6s^2}{1-0.2s}$) using MATLAB.
4. A) To generate the correlation of two signals using MATLAB.

   B) To generate sine, cosine and exponential function and generate correlation and convolution using MATLAB.
5. To plot and perform FFT and IFFT of sine signal using MATLAB.
6. To study effect of noise on signal and recover the original signal using MATLAB.
7. A) To plot amplitude and phase response of chebyshev filter 1 for analog input using MATLAB.

   B) To plot amplitude and phase response of chebyshev filter 2 for analog input using MATLAB.
8. A) To plot amplitude and phase response of chebyshev filter 1 for digital input using MATLAB.

   B) To plot amplitude and phase response of chebyshev filter 2 for digital input using MATLAB.

11. A) To plot amplitude and phase response of butterworth filter for analog input using MATLAB.

    B) To plot amplitude and phase response of butterworth filter for digital input using MATLAB.
12. A)To design FIR low pass filter using rectangular window technique.

    B) To design FIR high pass filter using rectangular window technique.

    C) To design FIR bandpass pass filter using rectangular window technique.

    D) To design FIR bandstop pass filter using rectangular window technique.

Course Outcomes: On successful completion of this course, the students should be able to:

- To generate frequency response of given system and given function using MATLAB.
- To generate sine, cosine and exponential function and generate correlation and convolution using MATLAB
- To plot amplitude and phase response of various filters for digital and analog input using MATLAB.
- To design FIR filters using rectangular window technique.

GO-705C **SWAMI VIVEKANANDA'S THOUGHTS**

L T P CR			
0 0 3 4	**External**	**:**	**75**
	Internal	**:**	**25**
	Total	**:**	**100**
	Duration of Exam	**:**	**3 Hrs.**

Course Objectives:

1. To introduce biography and philosophical thought of Swami Vivekananda
2. To present Swami Vivekananda's views on major religions of the world and Universal Religion
3. To present Swami Vivekananda' teaching and views on social issues.

Syllabus

Unit – 1

Swami Vivekananda – a Brief biography – Influence of Ramakrishna on Vivekananda – Parliament of Religions – Establishment of Ramakrishna mission.

Unit – 2

Philosophy of Swami Vivekananda - Nature of Reality , Nature of Self , Nature of the universe – The doctrine of Maya, Identity of Self and God, Karma Yoga, Raj Yoga , Bhakti Yoga, Gyan Yoga.

UNIT-3

Swami Vivekananda's observations on major religions of the world (a) Hinduism (b) Christianity (c) Islam

Unit - 4

The concept of Universal Religion and its characteristics – Fundamental unity of all religions – acceptance and not tolerance is the principle.

UNIT-5

Vivekananda and Nationalism – The message of patriotism – spirituality as the basis of patriotism, Sociological views of Vivekananda – His views on caste and untouchability - status of women – His views on Education – Swami Vivekananda's concept of Vedantic Socialism

Books:

1. The Complete Works of Swami Vivekananda Vol. 1 to 8 Relevant Chapters.